UNIT - 1

Introduction :

* The operational Amplifier most commonly referred as op-Amp was Introduced in 1940's. The first op-Amp was designed in 1948 using vaccum tubes. In those days, it was used in analog computers to perform variety of mathematical operations such as addition subtraction, multiplication etc.

* Due to use in performing mathematical operation. It has been given name op-Amp Due to use of vaccum tubes.

* The CKT design becomes very simple. The variety of useful circuits can be built without necessity of knowing about complex internal circuitie Moreover IC, op-Amp's are in expensive Take up less space and consume less power.

Advantages of IC :

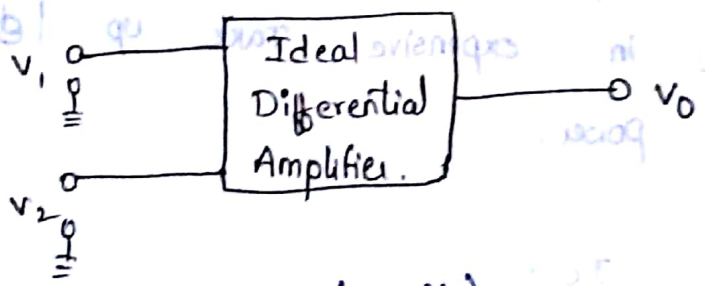
1. Low Cost
2. Small Size
3. Versalitly.
4. Flexibility
5. Dependability

Application of IC:

1. Process Control used IC's.
2. Communications.
3. Computers
4. power and signal source
5. Display and Meaning measuring System.
6. The op-Amp is basically building block of IC op-Amp. Thus let us study Diff. Amp and the supporting CKT's.

Basics of Differential Amplifier

Def: The Diff. Amp the Amplifies difference between two input voltage signals. Hence it is also called Differential Amplifier.



$$V_0 \propto (V_1 - V_2)$$

$$V_0 = A_d (V_1 - V_2)$$

where $A_d \rightarrow$ Diff. Gain

$V_d \rightarrow V_1 - V_2$.

$V_0 = A_d V_d$

Where $V_d \rightarrow$ Diff. B/w two i/p signals

$$A_d = \frac{V_o}{V_d} \quad \left(\because A_d = \frac{V_o}{V_{in}}\right).$$

$$A_d = 20 \log_{10} (A_d) \text{ in dB}$$

$$= 20 \log_{10} \left(\frac{V_o}{V_{in}}\right). \text{ in dB}$$

COMMON MODE GAIN:

* Suppose if we apply two i/p voltages which are Equal in all domains then ideally the o/p vltg $V_o = (V_1 - V_2) A_d$ is zero.

* It is practically not possible. The practical Diff. Amp not only depends on Diff. vltg but also depends on Avg. common level of three i/p's.

* Such an Avg. level of two i/p's called Common Mode Signal and it is denoted by

$$\boxed{V_c = \frac{V_1 + V_2}{2}}$$

The gain with which it is Amplifies Common Mode Signal to produce o/p is called Common Mode Gain of Amp. It is denoted as

$$V_o \propto V_c$$

$$V_o = A_c \cdot V_c$$

$A_c \longrightarrow$ Common Mode gain

If $V_1 = V_2$, There exist infinite o/p. Such common mode gain

Common Mode Rejection Ratio:

Definition:

The Ability of differential Amplifier to reject a common mode signal is expressed by ratio is CMRR.

It is defined as Ratio of Diff. vltg gain to common mode vltg gain.

$$CMRR = \rho = \frac{A_d}{A_c}$$

Ideally, common mode vltg gain zero. Hence the Ideal value of CMRR. is Infinite.

$$\rho = 20 \log \left[\frac{A_d}{A_c}\right] \text{ in dB.}$$

Output voltage in Terms of CMRR:

$$V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d}\right]$$

$$= A_d V_d \left[1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d}\right]$$

Features of Diff. Amp:

1. High Diff. vltg gain
2. Low Common Mode Gain
3. High CMRR.

4. Two i/p Terminals.

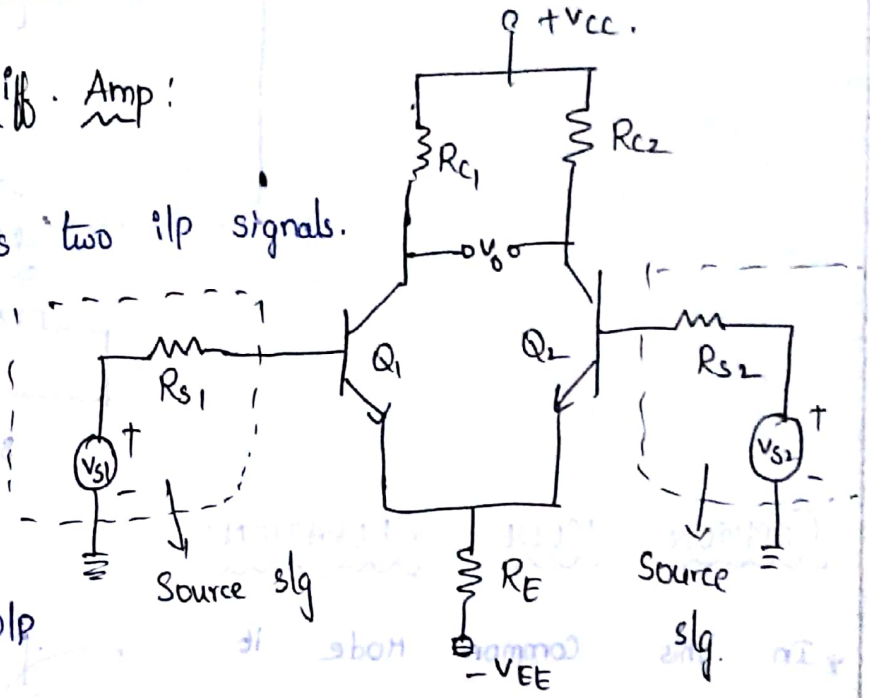
5. High i/p Impedance.

6. Large BW.

7. Low OFFset v/tgs & Currents.

8. Low o/p impedance.

Transistorized Diff. Amp:



* The CKT contains two i/p signals. there is no o/p Terminal will be GND

Then CKT called Dual i/p balanced o/p Diff. Amp.

It can be classified into 4 types depending on i/p & o/p's

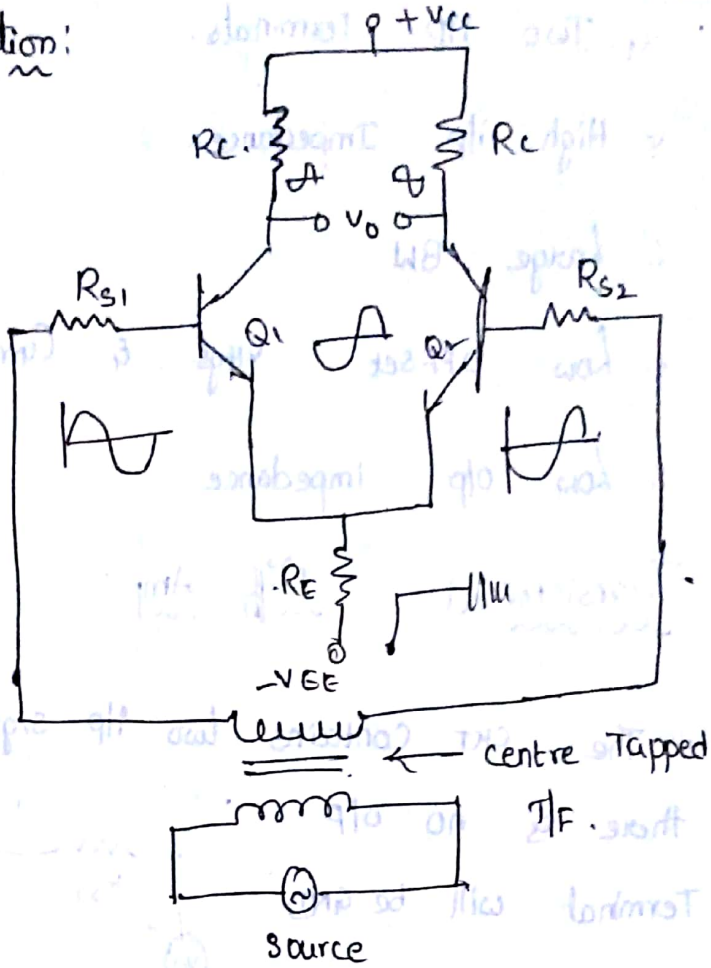
1. Dual i/p balanced o/p Diff. Amp
2. Dual i/p unbalanced o/p Diff. Amp
3. Single i/p balanced o/p Diff. Amp.
4. Single i/p unbalanced o/p Diff. Amp.

Dual i/p balanced o/p Diff. Amp:

The operation of CKT in 2 modes
1. Differential Mode operation
2. Common Mode operation

Differential Mode Operation:

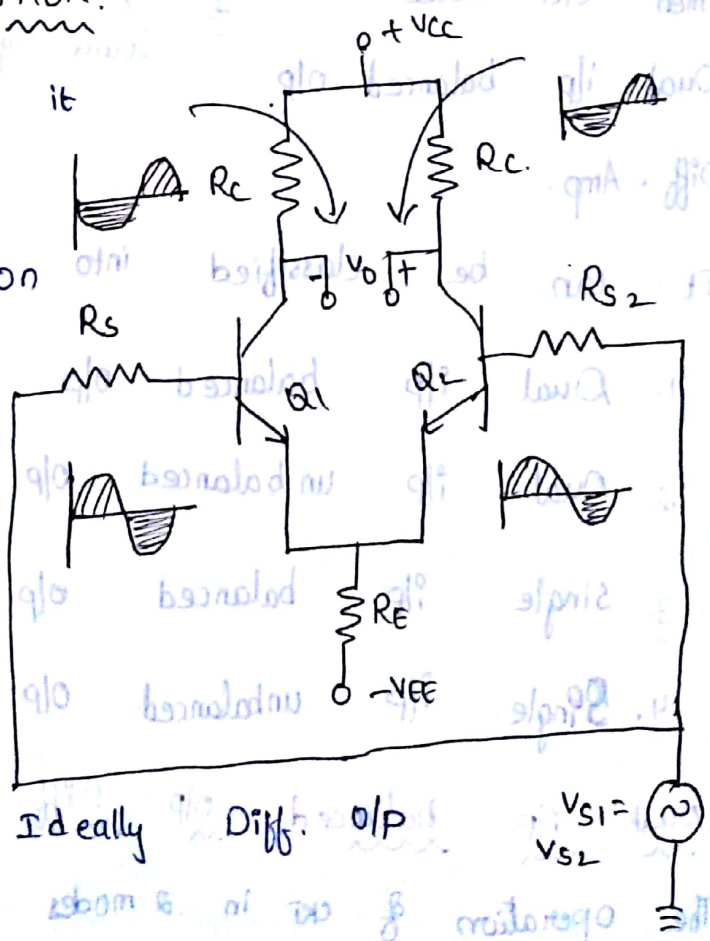
The Difference o/p V_0 is twice as large as signal vltg from Either Collector to ground.



COMMON MODE OPERATION:

* In this Common Mode it introduce -ve F/B this -ve F/B reduce Common Mode Gain

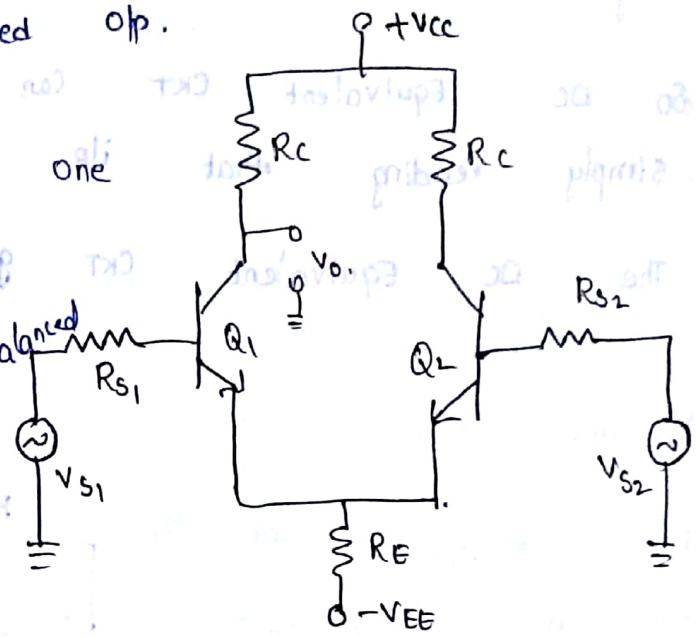
* In Common mode o/p vltg becomes zero.



Note: In Common Mode Ideally Diff. o/p is equal to zero.

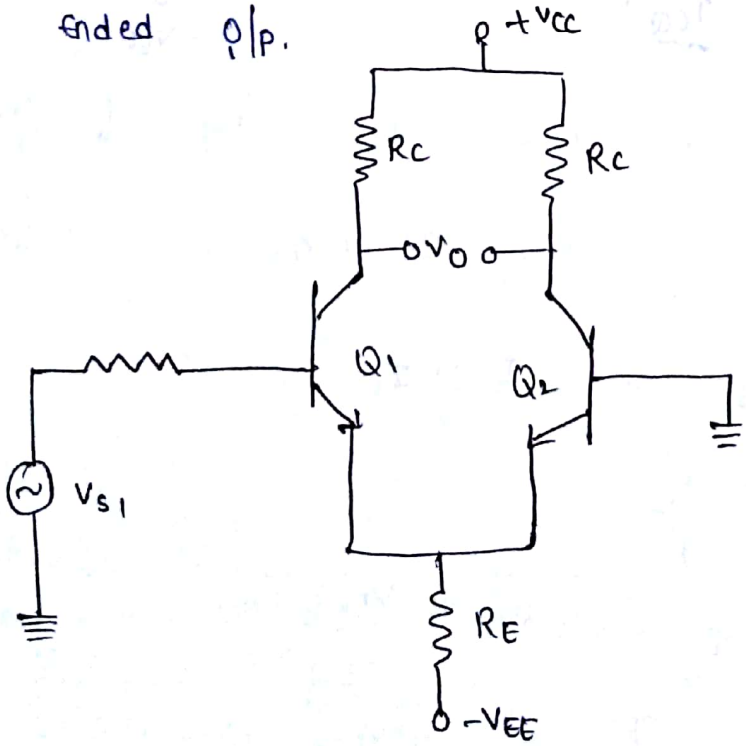
Dual Input unbalanced output differential Amplifier:

* If signal is given to both i/p terminal called Dual Input.
* If o/p is taken between two collectors called Balanced Output (or) Double Ended o/p.
* If o/p is taken btw one collector with respect to grounded called unbalanced o/p (or) Single ended o/p.



Single Input balanced output Differential Amplifier:

* If signal is given to only one i/p Terminal and other terminal is grounded is called single i/p single ended o/p.

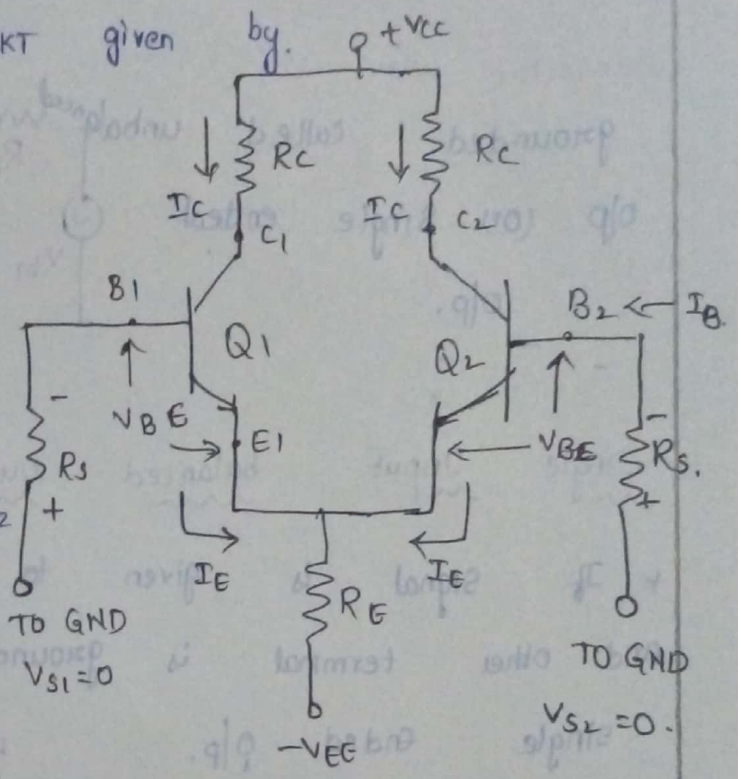


DC Analysis of Differential Amplifier:

* DC Analysis means operating point values that means, I_{CQ}, V_{CEQ} for Transistors used. The supply voltages are DC and i/p signals are AC.

* So DC Equivalent CKT can be obtained by simply reading that i/p AC signal to zero.

* The DC Equivalent CKT given by.



Assume $R_{S1} = R_{S2} = R_S$.

1. Two Transistor Q_1 and Q_2 are Same characteristics

2. $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \| R_{E2}$

3. $|V_{CC}| = |V_{EE}|$

Calculation of I_{CQ}:

Apply KVL to base Emitter loop of Q_1 Transistor

$$-I_B R_S - V_{BE} - 2 I_E R_E + V_{EE} = 0$$

W.K.T $I_C = \beta I_B$ and $I_C \simeq I_E$

$$\beta = \frac{I_E}{\beta}$$

$$-\frac{I_E R_S}{\beta} - V_{BE} - 2 I_E R_E + V_{EE} = 0$$

$$-I_E\left[\frac{R_S}{\beta} + 2R_E\right] - V_{BE} + V_{EE} = 0.$$

$$V_{EE} - V_{BE} = I_E \left[\frac{R_s}{\beta} + 2R_E \right]$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_s}{\beta} + 2R_E}$$

Generally $\frac{R_s}{\beta} <<< 2R_E$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

from this Eq^n.

1. R_E determines Emitter Current of Q_1 and Q_2 for known value of V_{EE}

2. The Emitter Current Q_1 and Q_2 is independent of Collector Resistance (R_C)

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{\frac{R_s}{\beta} + 2R_E} \simeq \frac{V_{EE} - V_{BE}}{2R_E}$$

Calculation of V_{CEQ}:

$$I_E \simeq I_C.$$

* If we know "I_E" $V_C = V_{CC} - I_C R_C$.

* Neglecting drop across "R_s" the voltage at Emitter Q_1 is approximately equal to $-V_{BE}$. Hence Collector to Emitter voltage is $V_{CE} = V_C - V_E$

$$= V_{CC} - I_C R_C - (-V_{BE})$$

$$\boxed{V_{CE} = V_{CEQ} = V_{CC} + V_{BE} - I_C R_C.}$$

* Hence $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$.

Neglect drop across "R_s" the voltage at Emitter of Q_1 is approximately equal to $-V_{BE}$. Hence collect to Emitter voltage

$$V_{EC} = V_C - V_E$$

$$= V_{CC} - I_C R_C - (-V_{BE})$$

$$= V_{CC} + V_{BE} - I_C R_C.$$

$I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CQE}$

* for given values of V_{CC} and V_{EE}

* The sign of V_{EE} is already consider to be Negative. There is no need to place negative sign to solve problem.

Common Mode Gain:

The magnitude of both AC i/p signal is V_s and there are in phase with each other. Hence differential i/p $V_d = 0$ while common mode i/p V_c is Avg. value of 2 i/p signals.

$$V_c = \frac{V_1 + V_2}{2}. \qquad V_c = V_s.$$

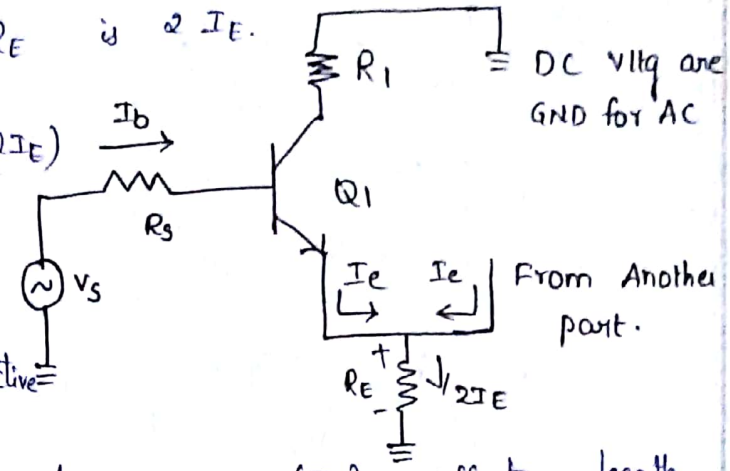
The o/p voltage given by

$$V_o = A_c V_c$$

$$= A_c V_s$$

$$\boxed{A_c = \frac{V_o}{V_s}}$$

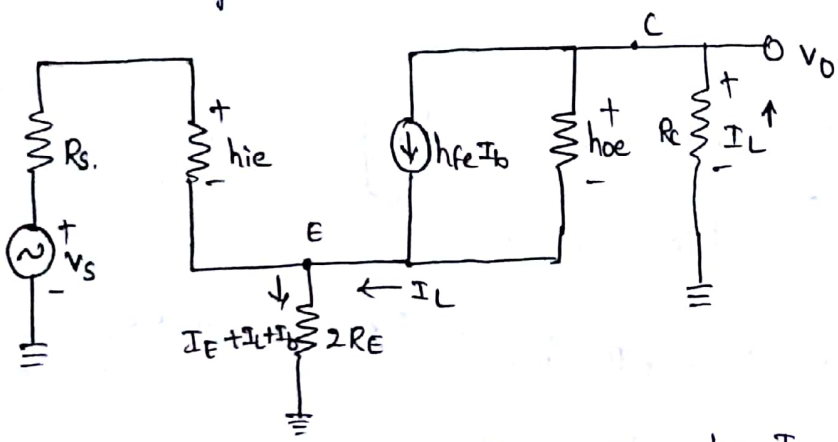
* The both Emitter Currents I_{E1} and I_{E2} is $I_{E1} = I_{E2} = I_E$ flow through R_E in same direction. Hence total Current flow through R_E is $2 I_E$.



* As Current through R_E is $(2I_E)$ For simplicity of derivation Current can be Assumed be I_B is and Emitter Effective

* So Current through R_C = load Current (I_L). Effective length Emitter resistance $= 2R_E$.

Current through Emitter Resistance $(I_E) = I_L + I_b$.



The Current through $h_{oe} = I_L - h_{fe} I_b$.

Apply KVL to i/p loop

$$-I_b R_S - I_b h_{ie} - 2R_E (I_L + I_b) + V_S = 0$$

$$V_S = I_b \left[R_S + h_{ie} + 2R_E \right] + I_L (2R_E) \quad \text{—— (1)}$$

W.K.T

$$V_O = -I_L R_C.$$

The Negative sign due to direction of Current KVL to o/p

$$-\frac{(I_L - h_{fe} I_b)}{h_{oe}} - 2R_E (I_L + I_b) - I_L R_C = 0.$$

$$-\frac{I_L}{h_{oe}} + \frac{h_{fe} I_b}{h_{oe}} - 2R_E I_L - 2R_E I_b - I_L R_C = 0$$

$$I_b\left(\frac{h_{fe}}{h_{oe}} - 2R_E\right) - I_L\left(\frac{1}{h_{oe}} + 2R_E + R_C\right) = 0.$$

$$I_b\left(\frac{h_{fe}}{h_{oe}} - 2R_E\right) = I_L\left(\frac{1}{h_{oe}} + 2R_E + R_C\right)$$

$$I_b\left(\frac{h_{fe} - 2R_E h_{oe}}{h_{oe}}\right) = I_L\left[\frac{1 + 2R_E h_{oe} + R_C h_{oe}}{h_{oe}}\right]$$

$$\frac{I_L}{I_b} = \frac{h_{fe} - 2R_E h_{oe}}{1 + (2R_E - R_C) h_{oe}} \quad \text{——— (2)}$$

Sub (2) in (1)

$$I_b = \frac{I_L\left[1 + (2R_E - R_C) h_{oe}\right]}{h_{fe} - 2R_E h_{oe}} \quad \text{——— (3)}$$

$$V_s = \frac{I_L\left[1 + (2R_E + R_C) h_{oe}\right](R_s + h_{ie} + 2R_E)}{h_{fe} - 2R_E h_{oe}} + I_L(2R_E)$$

Find LCM

$$\frac{V_s}{I_L} = \frac{1 + h_{oe}(2R_E + R_C)\left[R_s + h_{ie} + R_E(2)\right] + 2R_E\left[h_{fe} - 2R_E h_{oe}\right]}{h_{fe} - 2R_E h_{oe}}$$

$$= \frac{2R_E[1 + h_{fe}] + R_s[1 + 2R_E h_{oe}] + h_{ie}[1 + 2R_E h_{oe}] + h_{oe} R_C [2R_E + R_s + h_{ie}]}{h_{fe} - 2R_E h_{oe}}$$

Neglect $h_{oe} R_C << 1$.

$$\frac{V_s}{I_L} = \frac{2R_E(1+h_{fe}) + (1+2R_E h_{oe})(R_s + h_{ie})}{h_{fe} - 2R_E h_{oe}}.$$

Substitute value of I_L in "V_o".

$$V_o = -I_L R_c$$

$$= \frac{-V_s (h_{fe} - 2R_E h_{oe}) R_c}{2R_E(1+h_{fe}) + (1+2R_E h_{oe})(R_s + h_{ie})}$$

Common Mode Gain

$$A_c = \frac{V_o}{V_c}$$

$$= \frac{-V_s (h_{fe} - 2R_E h_{oe}) R_c}{V_s \left[2R_E(1+h_{fe}) + (1+2R_E h_{oe})(R_s + h_{ie})\right]}$$

Neglect hoe than Ac.

$$\boxed{A_c = \frac{-h_{fe} R_c}{2R_E(1+h_{fe}) + R_s + h_{ie}}} \rightarrow$$ Exp. for Common Mode Gain.

Common Mode Rejection Ratio:

The Ratio of Differential gain to common Mode gain

$$CMRR = \left|\frac{A_d}{A_c}\right|$$

$$= \frac{h_{fe} R_c}{R_s + h_{ie}} \times \frac{(R_s + h_{ie}) + 2R_E(1+h_{fe})}{-h_{fe} R_c}.$$

$$= \frac{(R_s + h_{ie}) + (2R_E(1+h_{fe}))}{R_s + h_{ie}}.$$

Differential Input Resistance:

It is Equivalent Resistance between one of i/p and ground then other i/p Terminal grounded.

$$R_i = \frac{V_s}{I_b}$$

W.K.T $I_b = \frac{V_s}{2(R_s + h_{ie})}$

From Diff. Gain KVL i/p loop $\frac{V_s}{I_b} = 2[R_s + h_{ie}]$

$$R_i = 2(R_s + h_{ie})$$

Output Impedance:

It is defined Equivalent resistance between one of o/p Terminals with respect to ground. from CKT resistance between the o/p Terminals with respect to Ground is R_c.

$\boxed{R_o = R_c}$. For all Configurations $R_o = R_c$.

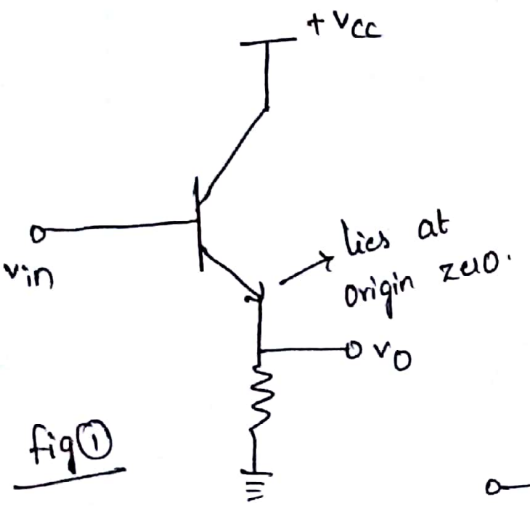
DC - Coupling Cascaded Differential Amplifier Stages:

Level Translator :

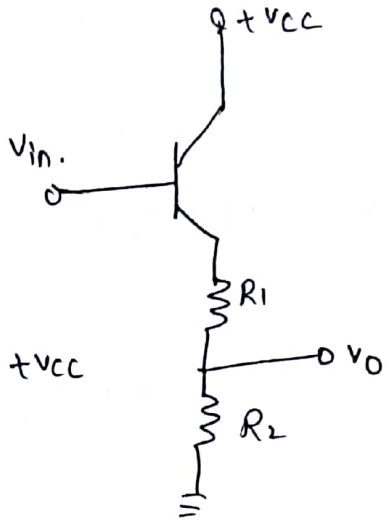
* Because of direct Coupling dc level rises from stage increases for AC level then tends for shift operating point of next stage.

* Hence o/p voltage swing may be distort and o/p will be minimized

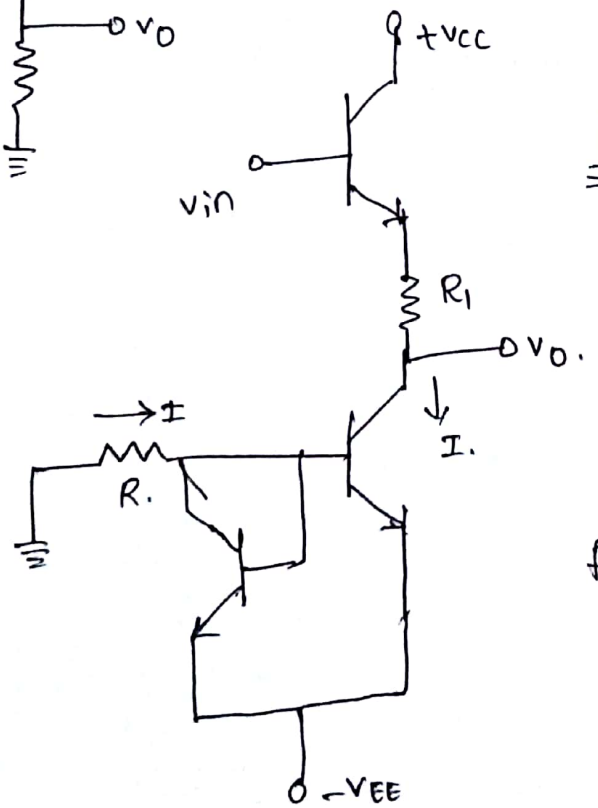
* The o/p should have Quiscent [Q point] voltage of zero will be i/p signal.



fig①



fig②



fig③

$V_o - V_{in} = -V_{BE} = -0.7\,V$

$V_o - V_{in} = -(V_B + IR_1)$

features of Level Translator:

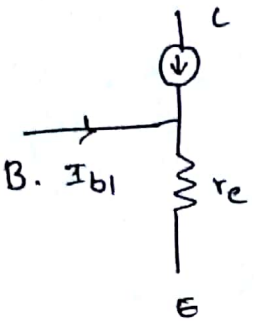
1. Wide Supply voltage Range.
2. Low propagation delay
3. Low power Suspended Mode
4. Auto Direction Sensing
5. Three State o/p operation
6. Over voltage Tolerance option

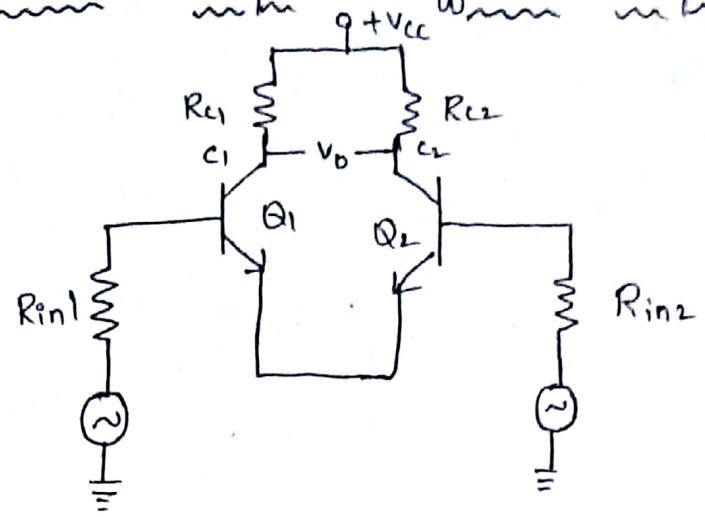
Applications:

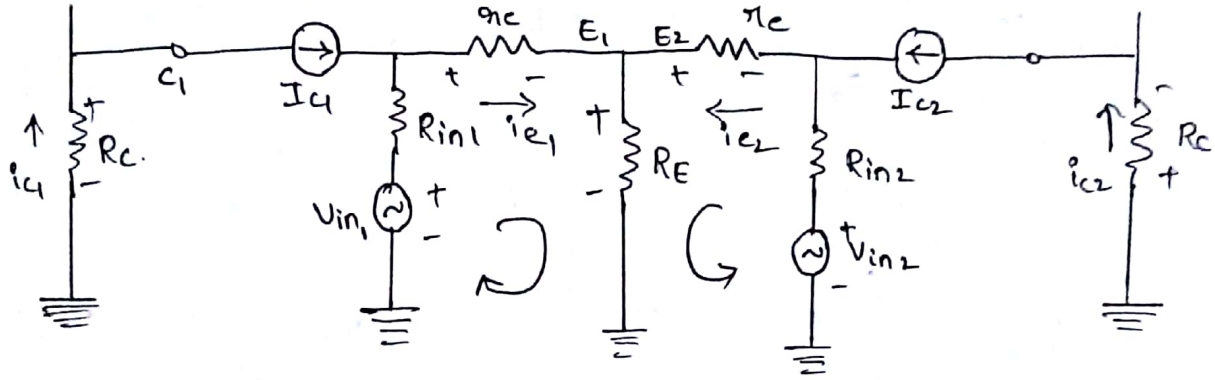
1. Cell phones
2. LCD TV
3. personal Computing

Dual Input Balanced Output Differential Amplifier:

Tϕ - Mode







For loop1: $V_{in1} - R_{in1} I_{b1} - I_{e1} r_e - R_E (i_{e1} + i_{e2}) = 0$.

for loop 2: $V_{in2} - R_{in2} I_{b2} - i_{e2} r_e - R_E (i_{e1} + i_{e2}) = 0$.

$$I_b = I_e / \beta_{ac} \qquad I_e = I_c$$

$$I_c = \beta I_b.$$

$$V_{in1} - R_{in1} \frac{I_{e1}}{\beta_{ac}} - I_{e1} r_e - R_E (i_{e1} + i_{e2}) = 0$$

$$V_{in2} - R_{in2} \frac{I_{e2}}{\beta_{ac}} - i_{e2} r_e - R_E (i_{e1} + i_{e2}) = 0$$

$$V_{in1} = i_{e1} \left(\frac{R_{in1}}{\beta_{ac}} + r_e + R_E \right) + i_{e2} R_E$$

$$V_{in2} = i_{e2} \left(\frac{R_{in2}}{\beta_{ac}} + r_e + R_E \right) + i_{e1} R_E$$

R_{in1} and R_{in2} are very small values here neglected.

$$V_{in1} = I_{e1}(r_e + R_E) + i_{e2} R_E$$

$$V_{in2} = I_{e2}(r_e + R_E) + i_{e1} R_E$$

$$\begin{bmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{bmatrix} \begin{bmatrix} i_{e1} \\ i_{e2} \end{bmatrix} = \begin{bmatrix} V_{in1} \\ V_{in2} \end{bmatrix}$$

$$i_{e1} = \frac{\begin{bmatrix} V_{in1} & R_E \\ V_{in2} & R_E + r_e \end{bmatrix}}{\begin{bmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{bmatrix}} = \frac{V_{in1}(r_e + R_E) - V_{in2} R_E}{(r_e + R_E)^2 - R_E^2}.$$

$$i_{e2} = \frac{\begin{bmatrix} r_e + R_E & V_{in1} \\ R_E & V_{in2} \end{bmatrix}}{\begin{bmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{bmatrix}} = \frac{V_{in2}(r_e + R_E) - V_{in1} R_E}{(r_e + R_E)^2 - R_E^2}.$$

$$V_o = V_{c2} - V_{c1}$$

$$= -R_c i_{e2} - (-R_c i_{c1})$$

$$= -R_c i_{e2} + R_c i_{e1}$$

$$V_o = R_c \left[\frac{V_{in1}(r_e + R_E) - R_E V_{in2}}{r_e^2 + 2 R_E r_e} - \frac{V_{in2}(r_e + R_E) - V_{in1} R_E}{r_e^2 + 2 R_E r_e} \right]$$

$$= R_c \left[\frac{(V_{in1} - V_{in2})(r_e + 2R_E)}{r_e (r_e + 2R_E)} \right] = \frac{R_c}{r_e} (V_{id}).$$

$$A = \frac{V_o}{V_{id}} = \frac{R_c}{r_e}.$$

Input Resistance:

$$R_{i_1} = \frac{V_{in1}}{i_{b1}}\Big|_{V_{in2}=0}$$

$$R_{i_1} = \frac{V_{in1}}{i_{e1}/\beta_{ac}}\Big|_{V_{in2}=0}$$

$$= \frac{\beta_{ac}\, V_{in1}}{i_{e1}}$$

$$= \frac{\beta_{ac}\, V_{in1}}{\dfrac{(r_e+R_E)V_{in1} - R_E V_{in2}}{(r_e+R_E)^2 - R_E^2}}\Bigg|_{V_{in2}=0}$$

$$= \frac{\beta_{ac}\, V_{in1}\,(r_e+R_E)^2 - R_E^2}{(r_e+R_E)\,V_{in1}} = \frac{\beta_{ac}\,(r_e+2R_E)\,r_e}{r_e+R_E}$$

$R_E \gg r_e$ So $(r_e + 2R_E) \simeq 2R_E$

$(r_e + R_E) \simeq R_E$

$$\boxed{R_{i_1} = \frac{\beta_{ac}\, r_e\, 2R_E}{R_E} = 2\beta_{ac}\, r_e}$$

$$R_{i_2} = \frac{V_{in2}}{i_{b2}}\Big|_{V_{in1}=0}$$

$$= \frac{\beta_{ac}\, V_{in2}}{\dfrac{(r_e+R_E)V_{in2} - R_E V_{in1}}{r_e^2 + 2r_eR_E}}\Bigg|_{V_{in1}=0}$$

$$R_{i_2} = \frac{\beta_{ac}\, V_{in2}\, r_e\,(r_e+2R_E)}{(r_e+R_E)\,V_{in2}}$$

$$R_{i_2} = \frac{\beta_{ac}\, r_e\,(r_e + 2R_E)}{(r_e + R_E)}$$

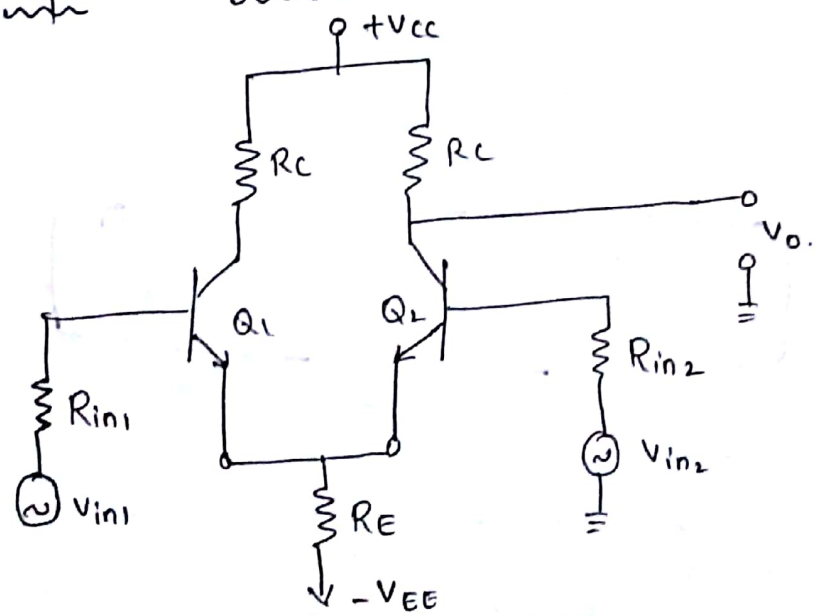
$$\boxed{R_{i_2} = \frac{\beta_{ac}\, r_e\, 2R_E}{R_E} \approx 2\beta_{ac}\, r_e}$$

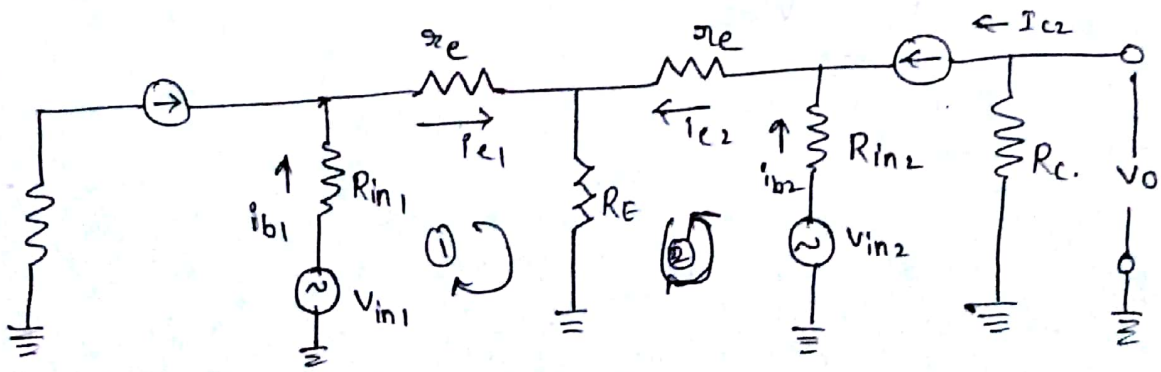
Output Resistance:

It is defined as equivalent resistance that would be measure at either of o/p terminal w.r.t ground Therefore the o/p resistance R_{o1} measured b/w the collector C_1 and ground and equal to R_{o2} measured at C_2 w.r.t equal to R_C. Thus

$$R_{o1} = R_{o2} = R_C$$

Dual - Input Unbalanced Output Differential Amplifier:





for loop 1 : $V_{in1} - R_{in1}\, i_{b1} - r_e\, i_{e1} - R_E(i_{e1} + i_{e2}) = 0$

$V_{in2} - R_{in2}\, i_{b2} - r_e\, i_{e2} - R_E(i_{e1} + i_{e2}) = 0$

$$i_{b1} = \frac{i_{e1}}{\beta_{ac}} \qquad i_{b2} = \frac{i_{e2}}{\beta_{ac}}$$

$$V_{in1} = i_{e1}\left[\frac{R_{in1}}{\beta_{ac}} + r_e + R_E\right] + R_E\, i_{e2}.$$

$$V_{in2} = i_{e2}\left[\frac{R_{in2}}{\beta_{ac}} + r_e + R_E\right] + R_E\, i_{e1}.$$

$$\begin{bmatrix} V_{in1} \\ V_{in2} \end{bmatrix} = \begin{bmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{bmatrix} \begin{bmatrix} i_{e1} \\ i_{e2} \end{bmatrix}$$

$$i_{e1} = \frac{\begin{bmatrix} V_{in1} & R_E \\ V_{in2} & R_E + r_e \end{bmatrix}}{\begin{bmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{bmatrix}} = \frac{V_{in1}(r_e + R_E) - V_{in2} R_E}{(r_e + R_E)^2 - R_E^2}$$

$$i_{e2} = \frac{\begin{bmatrix} r_e + R_E & V_{in1} \\ R_E & V_{in2} \end{bmatrix}}{\begin{bmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{bmatrix}} = \frac{V_{in2}(r_e + R_E) - V_{in1} R_E}{(r_e + R_E)^2 - R_E^2}$$

$$V_o = -R_C\, i_{C2} = -R_C\, i_{e2}.$$

$$V_o = -R_C\left[\frac{V_{in2}(r_e + R_E) - V_{in1} R_E}{r_e^2 + 2R_E r_e}\right]$$

$$= +\frac{R_C}{r_e}\left[\frac{V_{in1}(R_E) - V_{in2}(R_E)}{2R_E}\right]$$

$$V_0 = \frac{R_C}{r_e}\left[\frac{V_{in_1} R_E - V_{in_2} R_E}{2R_E}\right]$$

$$= \frac{R_C R_E}{2 r_e R_E}\left[\frac{V_{in_1} - V_{in_2}}{2R_E}\right]$$

$$= \frac{R_C}{2 r_e} V_{id}$$

$$\boxed{\frac{V_0}{V_{id}} = \frac{R_C}{2 r_e} = A}$$

Input Resistance :

$$R_{i_1} = \frac{V_{in_1}}{i_{b_1}}\Bigg|_{V_{in_2}=0}.$$

$$R_{i_1} = \frac{V_{in_1}}{i_{e_1}/\beta_{ac}}\Bigg|_{V_{in_2}=0} = \frac{\beta_{ac} V_{in_1}}{i_{e_1}}\Bigg|_{V_{in_2}=0}$$

$$= \frac{V_{in_1}\beta_{ac}(r^2 + 2R_E r_e)}{V_{in_1}(r_e+R_E) - V_{in_2}R_E}\Bigg|_{V_{in_2}=0}$$

$$= \frac{\beta_{ac} r_e (r_e + 2R_E)}{(r_e + R_E)}$$

$$= \frac{2\beta_{ac} r_e R_E}{R_E} = 2\beta_{ac} r_e.$$

$$R_{i_2} = \frac{V_{in_2}}{i_{b_2}}\Bigg|_{V_{in_1}=0}$$

$$= \frac{V_{in_2}\beta_{ac}}{i_{e_1}}\Bigg|_{V_{in_1}=0} = \frac{V_{in_2}\beta_{ac}(r^2 + 2R_E r_e)}{V_{in_2}(r_e+R_E) - V_{in_1}R_E}\Bigg|_{V_{in_1}=0}$$

$$R_{i2} = \frac{V_{in2}\,\beta_{ac}\, r_e\,(r_e + 2R_E)}{V_{in2}\,(r_e + R_E)}$$

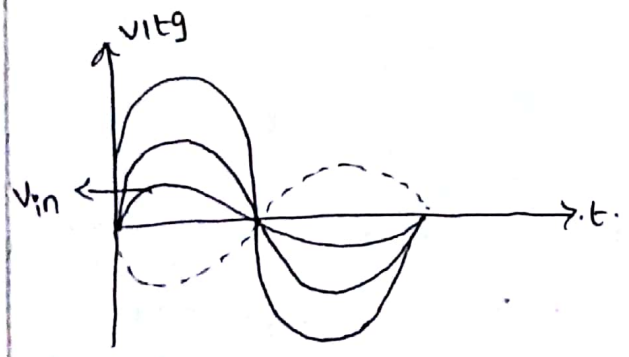
$$= \frac{\beta_{ac}\, r_e\, 2R_E}{R_E} = 2\, r_e\, \beta_{ac}$$

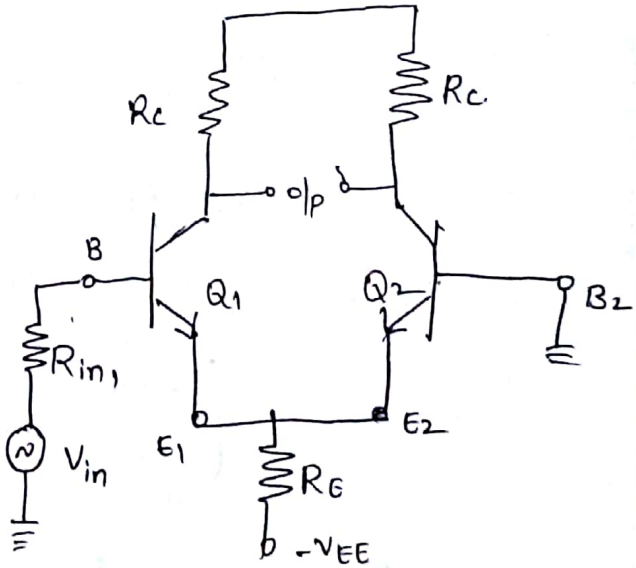
Output Resistance:

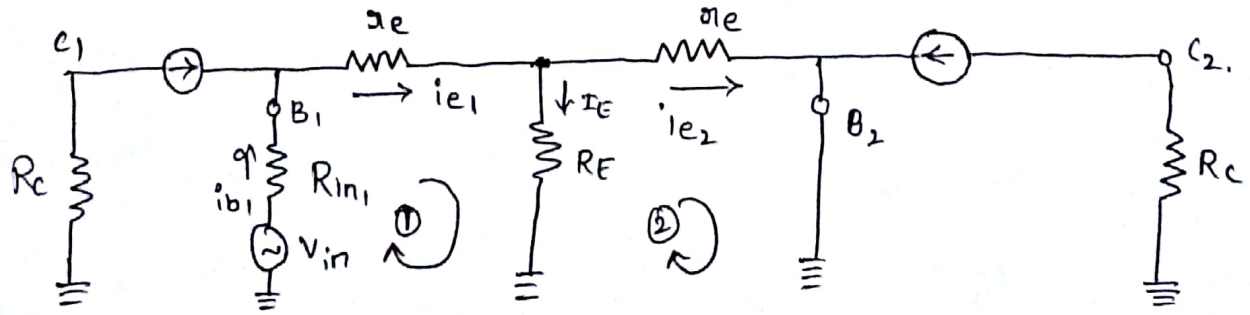
* The o/p resistance R_o measured at C_2 w.r.t. GND and Equal to collector Resistor R_c.

$$\boxed{R_o = R_c.}$$

Single Input, Balanced output Differential Amp







Loop 1 : $V_{in1} - R_{in1} i_{b1} - r_e i_{e1} - R_E i_e = 0$

Loop 2 : $V_{in1} - R_{in1} i_{b1} - r_e i_{e1} - r_e i_{e2} = 0$

$$V_{in_1} - \frac{R_{in_1} i_{e1}}{\beta_{ac}} - r_e i_{e1} - R_E (i_{e1} + i_{e2}) = 0$$

$$V_{in_1} - \frac{R_{in_1} i_{e1}}{\beta_{ac}} - r_e i_{e1} - r_e i_{e2} = 0.$$

$$V_{in_1} - r_e i_{e1} - R_E (i_{e1} - i_{e2}) = 0$$

$$V_{in_1} - r_e i_{e1} - r_e i_{e2} = 0.$$

$$\begin{bmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{bmatrix} \begin{bmatrix} i_{e1} \\ i_{e2} \end{bmatrix} = \begin{bmatrix} V_{in_1} \\ V_{in_1} \end{bmatrix}$$

$$i_{e1} = \frac{\begin{bmatrix} V_{in_1} & -R_E \\ V_{in_1} & r_e \end{bmatrix}}{\begin{bmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{bmatrix}} = \frac{V_{in_1} r_e + V_{in_1} R_E}{r_e (r_e + R_E) + R_E r_e}.$$

$$i_{e2} = \frac{\begin{bmatrix} r_e + R_E & V_{in_1} \\ r_e & V_{in_1} \end{bmatrix}}{\begin{bmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{bmatrix}} = \frac{(r_e + R_E) V_{in_1} - r_e V_{in_1}}{r_e (r_e + R_E) + R_E r_e}.$$

$$i_{e2} = \frac{V_{in_1} R_E}{r_e (r_e + 2R_E)}$$

$$V_0 = V_{C2} - V_{C1}$$

$$= R_C i_{C2} - (-R_C i_{C1})$$

$$= R_C [i_{C2} + i_{C1}]$$

$$v_0 = R_C [i_{e2} + i_{e1}]$$

$$V_o = R_C \left[\frac{V_{in1} R_E}{r_e(r_e + 2R_E)} + \frac{V_{in1}(r_e + R_E)}{r_e(r_e + 2R_E)} \right]$$

$$= \frac{R_C}{r_e} \left[\frac{V_{in1}(r_e + 2R_E)}{r_e + 2R_E} \right] = \frac{R_C}{r_e} \times V_{in1}$$

$$A = \frac{V_o}{V_{in1}} = \frac{R_C}{r_e}.$$

Input Resistance:

$$R_i = \frac{V_{in1}}{i_{e1}/\beta_{ac}}$$

$$= \frac{\beta_{ac} V_{in1} (r_e(r_e + 2R_E))}{V_{in1}(r_e + R_E)}$$

$$= \frac{\beta_{ac} r_e (r_e + 2R_E)}{(r_e + R_E)}$$

$R_E >> r_e$ $\quad r_e + 2R_E \simeq 2R_E$

$r_e + R_E \simeq R_E$

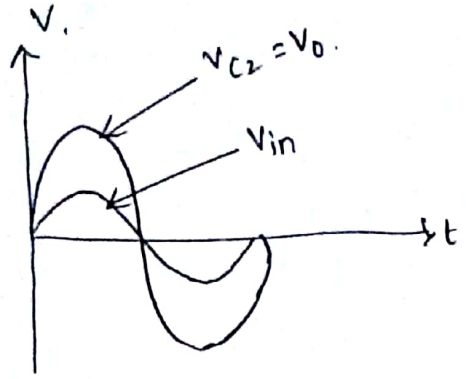
$$R_i = \frac{\beta_{ac} r_e 2R_E}{R_E} = 2\beta_{ac} r_e.$$

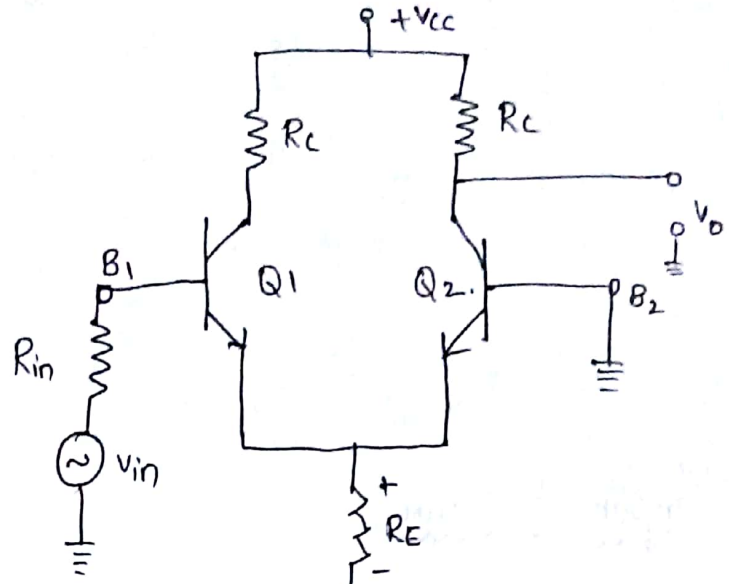
Output Resistance:

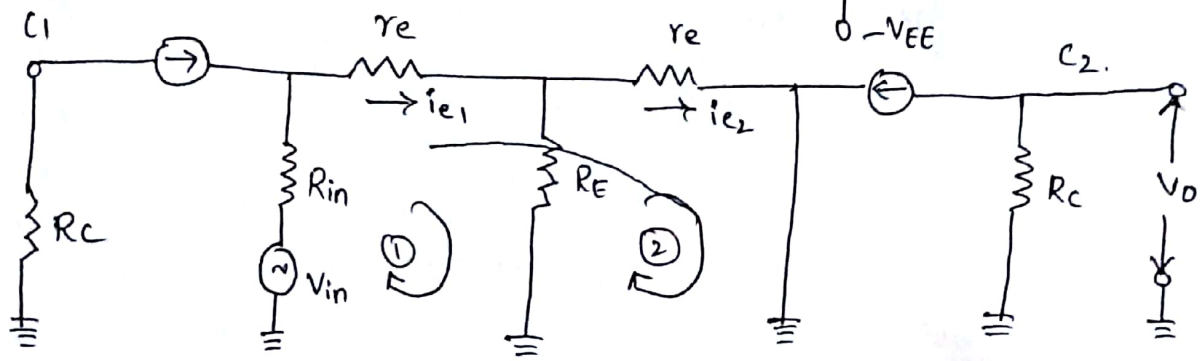
* The Output Resistance R_o is equivalent Resistance that would be measured at Either o/p Terminal w.r.t ground. Therefore o/p Res. R_{o1} measured at C_1 and R_{o2} measured at C_2

$$\boxed{R_{o1} = R_{o2} = R_C}$$

Single Input Unbalanced Output Differential Amplifier:







Loop 1: $V_{in} - R_{in}\, i_{b1} - r_e\, i_{e1} - R_E I_E = 0$

Loop 2: $V_{in} - R_{in}\, i_{b2} - i_{e1} r_e + i_{e2} r_e = 0$

$$V_{in} - \frac{R_{in}\, i_{e1}}{\beta_{ac}} - r_e\, i_{e1} - R_E I_E = 0$$

$$V_{in} - \frac{R_{in}\, i_{e1}}{\beta_{ac}} - r_e\, i_{e1} - i_{e2} r_e = 0$$

$$V_{in} - r_e\, i_{e1} - R_E (I_{e1} - i_{e2}) = 0$$

$$V_{in} - r_e\, i_{e1} - r_e\, i_{e2} = 0.$$

$$\begin{bmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{bmatrix} \begin{bmatrix} i_{e1} \\ i_{e2} \end{bmatrix} = \begin{bmatrix} V_{in} \\ V_{in} \end{bmatrix}$$

$$i_{e_1} = \frac{\begin{vmatrix} V_{in} & -R_E \\ V_{in} & r_e \end{vmatrix}}{\begin{vmatrix} r_e+R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{V_{in}\,(r_e+R_E)}{r_e\,(r_e+R_E2)}$$

$$i_{e_2} = \frac{\begin{vmatrix} r_e+R_E & V_{in} \\ r_e & V_{in} \end{vmatrix}}{\begin{vmatrix} r_e+R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{(r_e+R_E)\,V_{in} - r_e\,V_{in}}{r_e\,(r_e+R_E) + R_E\,r_e}$$

$$= \frac{V_{in}\,R_E}{r_e(r_e+2R_E)}$$

$$V_o = +R_C\,i_{c_2}$$

$$= R_C\,i_{e_2}$$

$$= R_C\left[\frac{V_{in}\,R_E}{r_e(r_e+2R_E)}\right] = \frac{V_{in}\,R_E\,R_C}{r_e\,(2R_E)}$$

$$\boxed{A_v = \frac{V_o}{V_{in}} = \frac{R_C}{2r_e}}$$

Input Resistance:

$$R_i = \frac{V_{in}}{i_{b_1}} = \frac{\beta_{ac}\,V_{in}\,r_e\,(r_e+2R_E)}{V_{in}\,(r_e+R_E)}$$

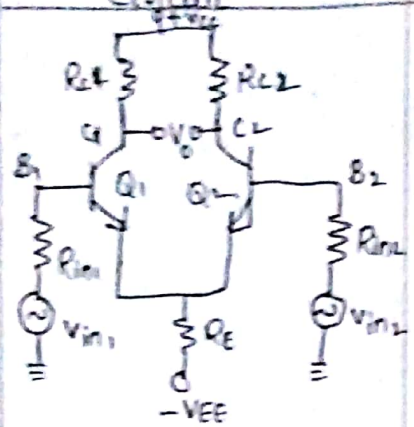
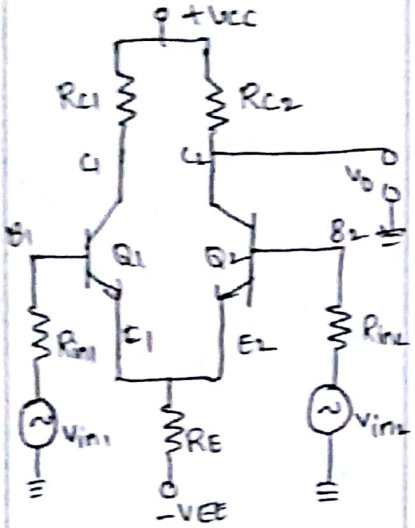
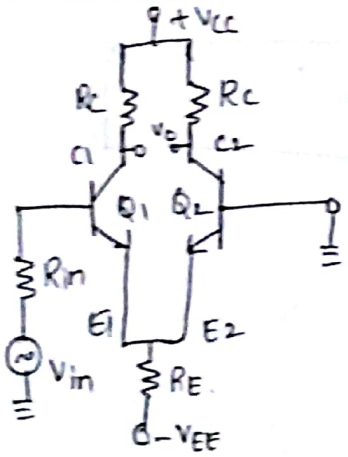
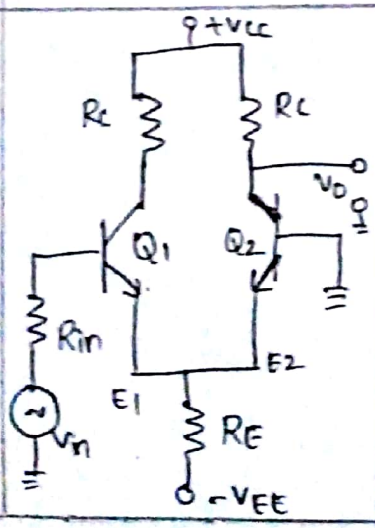
$$= \frac{\beta_{ac}\,r_e\,(2R_E)}{R_E} = 2\beta_{ac}\,r_e.$$

Output Resistance:

* The Output Resistance R_o is measured at Collector C_2 W.r.t GND and is equal to R_C.

$$\boxed{R_o = R_C}$$

Properties of Differential Amplifier.

Configuration	Circuit	Voltage Gain	I/P Resistance	O/P Resistance
Dual i/p Balanced o/p Diff. Amp.		$A = \frac{R_c}{r_e}$	$R_i = 2\beta_{ac} r_e$	R_c
Dual i/p Unbalanced o/p Diff. Amplifier		$A = \frac{R_c}{2r_e}$	$2\beta_{ac} r_e$	R_c
Single i/p Balanced o/p Diff. Amp.		$\frac{R_c}{r_e}$	$2\beta_{ac} r_e$	R_c
Single i/p unbalanced o/p Diff. Amp.		$\frac{R_c}{2r_e}$	$2\beta_{ac} r_e$	R_c

UNIT-II

INTEGRATED CIRCUITS [CONTINUATION]

Operational Amplifier:

The CKT, which perform mathematical operations like addition subtraction, multiplication then CKT is known as operational Amplifier. It is also known as OP-Amp.

Characteristics of OP-Amp:

1. Input off-set voltage.
2. Input off-set Current.
3. Input Bias Current.
4. Differential Input Resistance.
5. Input Capacitance.
6. Open Loop Voltage Gain.
7. Common Mode Gain Rejection Ratio. [CMRR]
8. Output Voltage Swing
9. Output Resistance
10. OFF set Voltage adjustment Range
11. Input Voltage Range.
12. power Supply Rejection Range Ratio
13. power Consumption
14. Slew-Rate
15. Gain Bandwidth product.

16. Equivalent i/p Noise voltage and Current.

17. Average Temperature Coefficient of OFF-set parameters

18. Output OFF-set voltage.

19. Supply Current.

Advantage of IC Technology:

1. It is in small size.
2. Low cost
3. Less weight
4. Low supply voltages
5. Low power consumption
6. Highly realiable
7. Matched Devices
8. fast speed.

Classification of IC's:

* IC's are two Types i) Digital IC ii) Linear IC.

Digital IC:

* The IC's which uses Logic Gates & implementation of Logical operations are Digital IC's.

Linear IC:

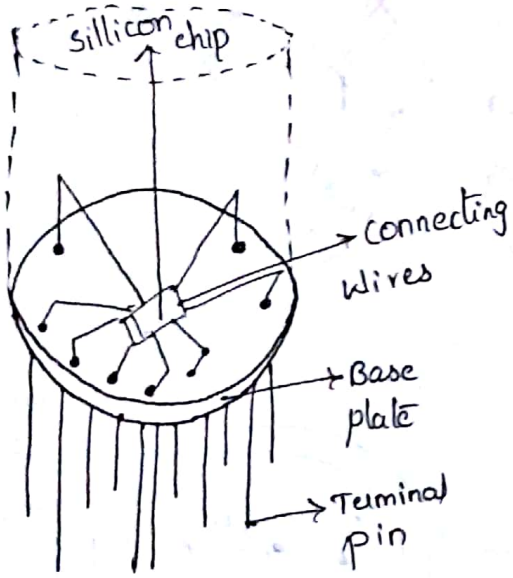
* The IC which user resistor, capacitor etc and the implement a Linear CKT are called Linear IC.

Classification of IC's:

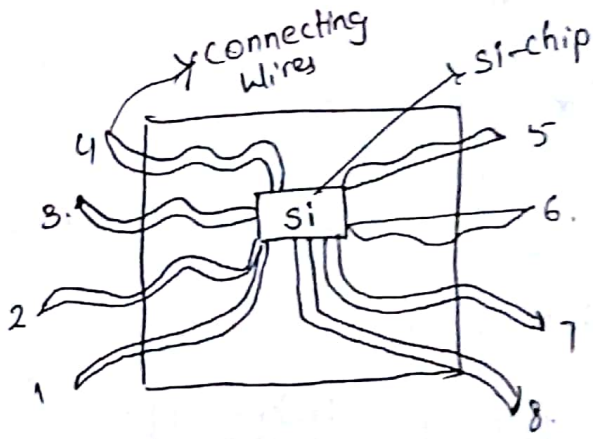
Integrated Circuits

- Mono lithic
  - Bipolar [BJT]
    - Using PN Junction Isolation
    - Using dielectric Isolation
  - Unipolar [FET]
    - MOSFET
    - JFET
- Thick & Thin
- Hybrid.

a) Monolithic IC in can - Type Enclosure :



b) plastic package Type :



* The word Monolithic originated from Greek word and it means " Single Stone / one stone ".

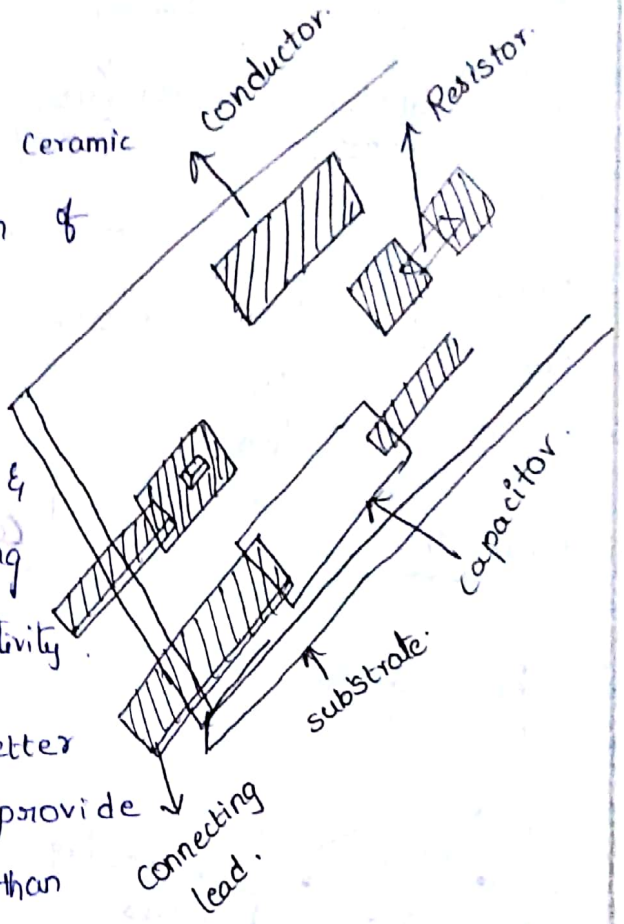
* In this all active as well passive Components along with Inter Connections are integrated on single crystal

* The Various processors involved in fabrication of different devices are Carried out in single plane.

* Hence this also referred as planar Technology

Monolithic IC's are referred for applications in which identical electronic CKTs are require in large number.

Thick and Thin film Technology:

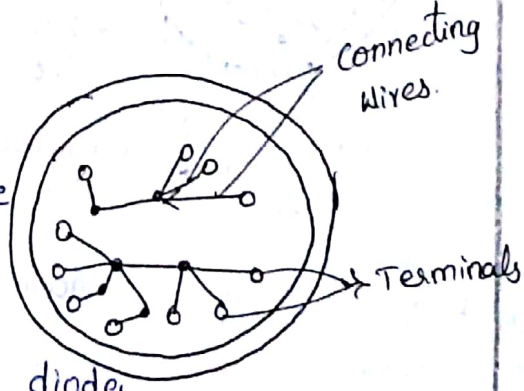


* In thin film IC glass are ceramic surface used to deposit film of conducting material.

* Here, resistor & conductors are fabricated by controlling width & Thickness of films and by using different materials for their restivity.

* Using, Technology, it have better Component tolerance and they provide better high freq. preformance than Monolithic Integrated Circuits.

Hybrid Technology:



* Hybrid are multi-chip IC constructe by interconnection no. of individual chips

* The active Components are diffused diodes

* The passive components are diffused Res. / capacitor on single chip. The connection b/w chips are provided by wiring / metalised patterns.

COMPARISION OF IC families :

IC family Properties	Monolithic - IC	Thick & Thin film IC	Hybrid IC
Substrate	Sillicon	Glass Ceramic	Glass, ceramic, Si
Structure	1. Active & passive device along with the interconnection on a single chip.	1. Active & passive devices on insulating substrate along with inter connection	1. Passive devices & interconnection on one insulating sub with active devices wire bound. 2) Active devices on single chip while passive device along with inter connection on Thick Thin film.
Active devices.	1. BJT 2. MOSFET	1. MOSFET	1. BJT 2. MOSFET.
Passive Devices.	1. Diffused Resistor, Oxite Capacitor. Mos Resistor, Oxite Capacitor.	1. Metal film resistor, oxite Capacitor.	1. Metal film res, Cement resistor, Oxite Capacitor. 2) Metal film resistor Oxite Capacitor.
Applications	Linear and Digital IC circuits	Digital IC Circuits.	Linear and Digital IC circuits

IC chip Size and Circuit Complexity :

S.NO	Level of Integration	No. of active devices for chip.
1.	Small Scale Integration	Less than 100
2.	Medium Scale Integration	100 – 10,000
3.	Large scale Integration	1000 – 100,000
4	Very large Scale Integration	Over 100,000.
5.	Ultra large Scale Integration	Over 1 Million

Package Types and Temperature Ranges :

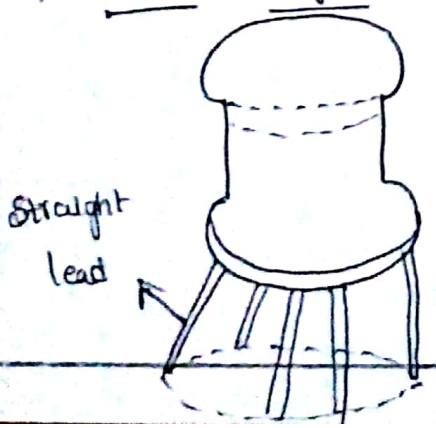
Package Types :

The OP-Amp IC's are available in various packages. The IC's package are classified into 3 Types.

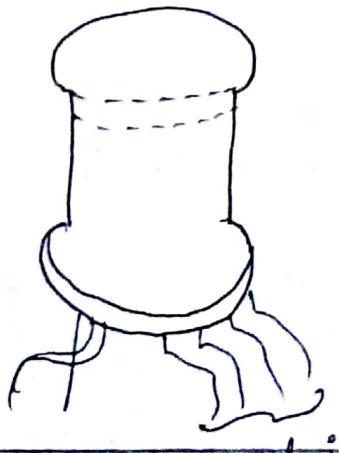
1. Metal Can (TO)
2. Dual - in - line (DIP)
3. Flat - Top - pack.

Metal Can package :

a) TO - 5 style Package

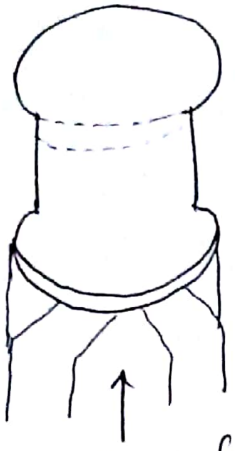


b) TO - 5 style pack [8 lead]



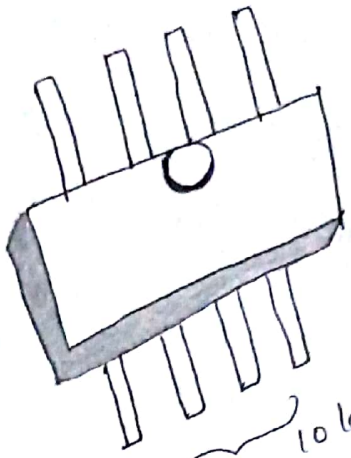
Dual in line

2). TO-5 style Package:



Radial formed leads.

Ceramic flat Package:



10 lead version

Selection of IC packages.

Types	Criteria.
Metal Can package	1. Heat Dissipation is important. 2. For high power App. like power Amp, Vltg Reg
Dual-in-line package.	1. for experimental (Bread Boarding purpose as easy to mount. 2. If bending (soldering of leads not Required 3. Suitable printed CKT points as lead spacing more
Flat package	1. More Reliability Required. 2. Light in weight. 3. Suited for air borne Applications.

Factors Effecting Selection of IC package:

1. Relative Cost.
2. Realiability
3. Weight of Package.

4. Ease of IC fabrication
5. power to be dissipated
6. Need of External heat sinks.

Temperature Ranges:

* There are three different Temperature Grades based on which OP-Amp IC's are classified. These Temp ranges are given below.

i) Millitary Temperature Range — [-55°c to +125°c] or [-55°c to +85°c]

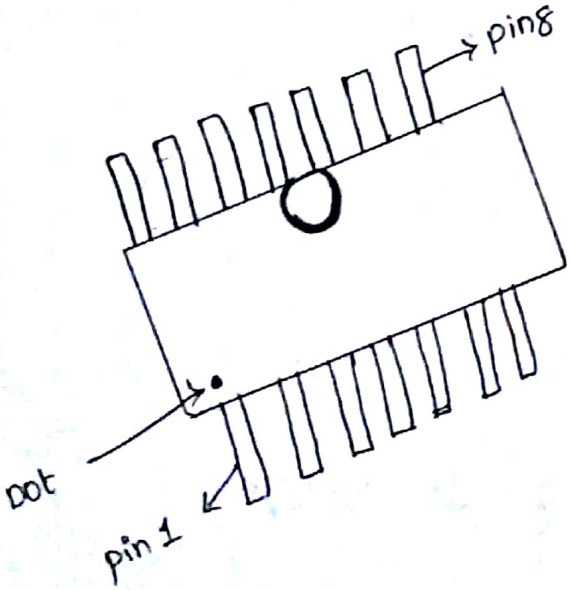
ii) Industrial Temperature Range — [-20°c to +85°c] or [-40°c to +85°c]

iii) Commercial Temperature Range — [0°c to +70°c] or [0°c to 75°c]

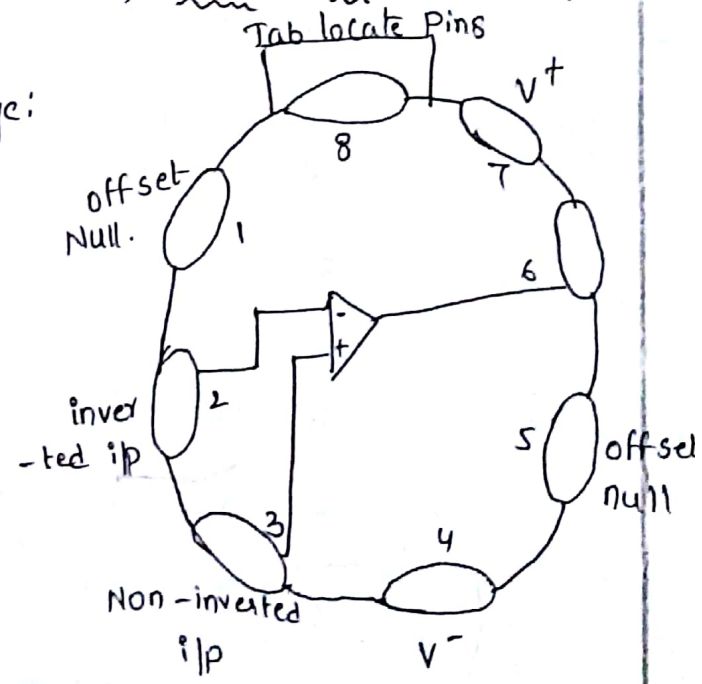
Pin - Identification:

Ceramic flat Package:

a) 14-lead version flat package:

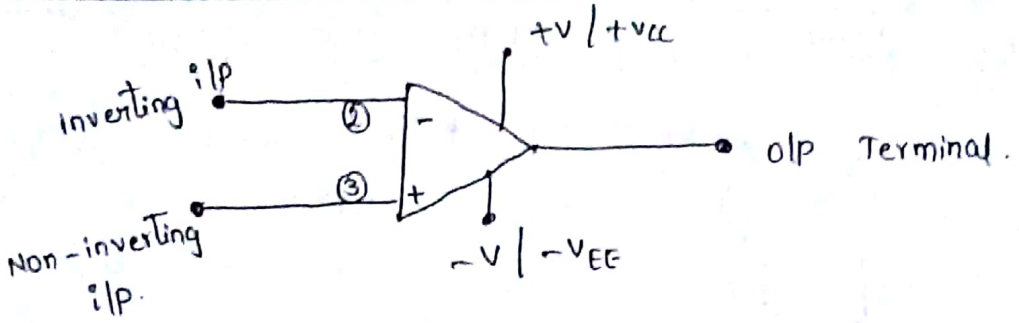


b) Metal - Can package:



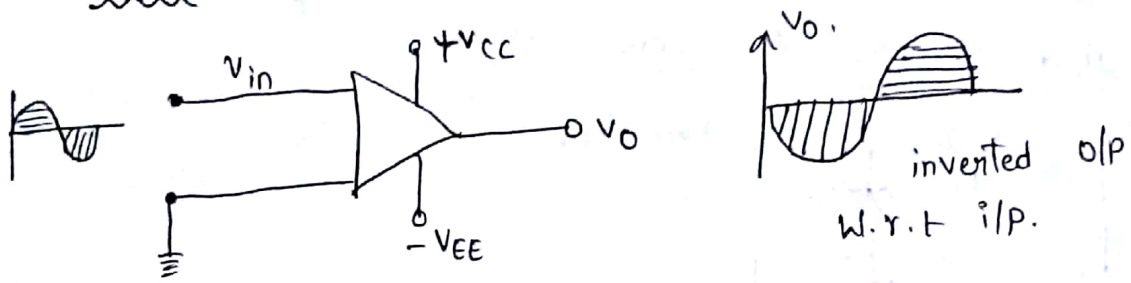
OP-Amp symbol and Terminals:

OP-Amp Symbol:

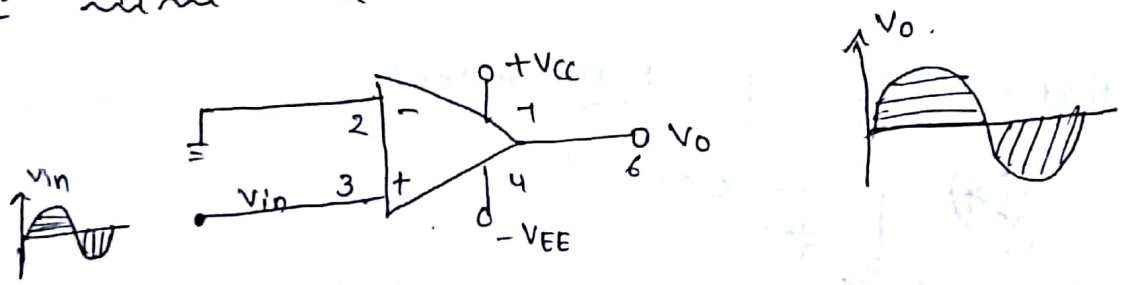


Case (i):

Input Applied to Inverting Terminal:

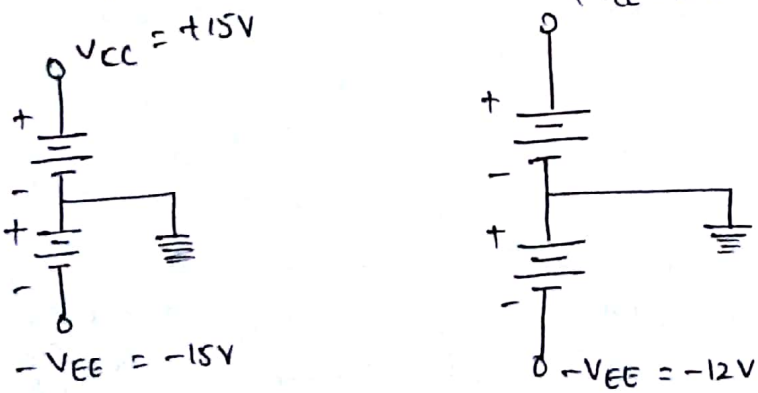


Input Applied to Non-Inverting Terminal:



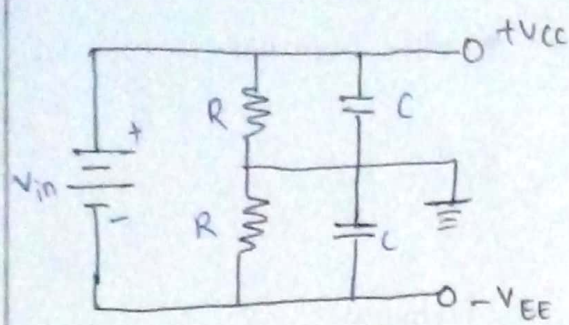
Power Supplies:

OP-Amp Works on dual Supply
1. positive supply voltage
2. Negative supply voltage



a) Balanced Supply voltage b) Unbalanced Supply voltage

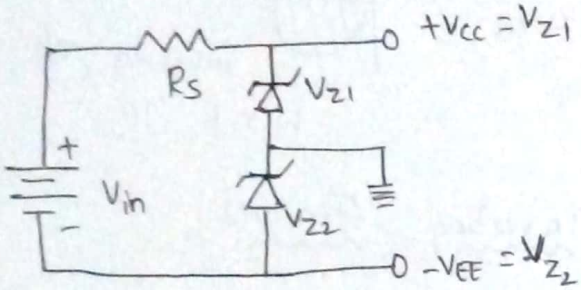
Obtaining Dual Supply from Single Supply :



* There are various methods to obtain Dual supply from Single supply. The above represents resistive protection divider Network and GND.

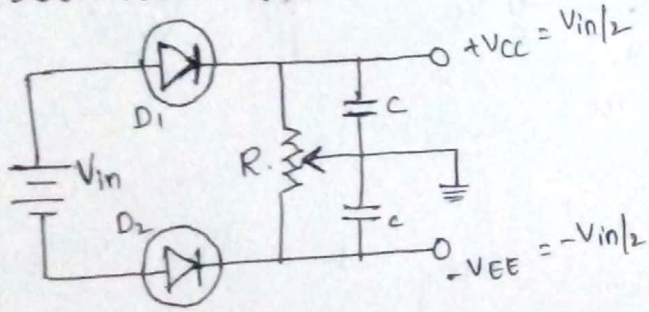
It is Converted to Dual supply.

Method 2 : Use of Zener Diode :



1. Practically, Due to mismatch in devices equal to +ve & -ve voltages are not available.
2. To adjust them potentiometer can be used.

Method 3 : Use of potentiometer :



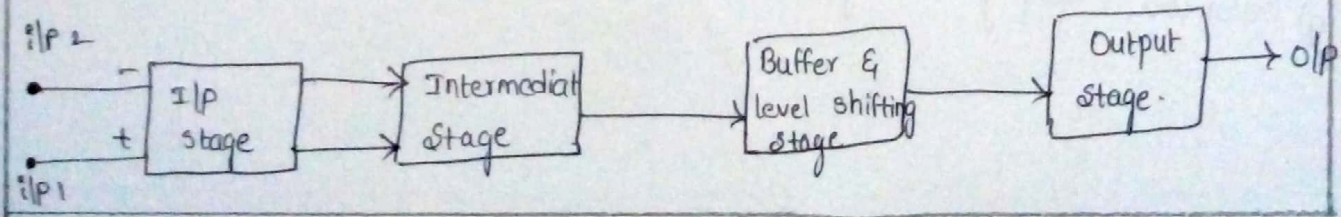
To avoid damage due to reversal of polarities connected to IC diode D_1 and D_2 can be used.

Block diagram of OP-Amp :

* W.K.T Now-a-days, OP-Amp's are available in an IC CKT form

The Commercial Integrated CKT OP-Amp usually consists of 4 Cascaded blocks

The block diagram of IC OP-Amp given by



Input Stage :

* The basic requirements of i/p stage of op-Amp

1. High voltage Gain
2. High input impedance.
3. Two input Terminals
4. Small input OFF-set voltage
5. Small input OFF set Current.
6. High CMRR.
7. Low i/p bias Current.

* Dual i/p balanced o/p Differential Amp satisfies all these requirement. Hence Commonly used i/p stage.

* It provides 2 i/p Terminals, Inverting & Non-inverting and it provide high voltage Gain.

INTERMEDIATE STAGE :

* The o/p of i/p stage drives next stage which is an Intermediate stage.

* In this Intermediate stage another differential Amp. with dual i/p unbalanced o/p [single Ended o/p] is used.

* The Overall gain Requirement of op-Amp is very high. The i/p stage alone Cannot provide such a high Gain.

* The main function of Intermediate stage is to provided additional vltg gain required.

* Thus requirements of Intermediate stage are

1. Very high Voltage Gain
2. Direct coupling without Coupling Capacitors.

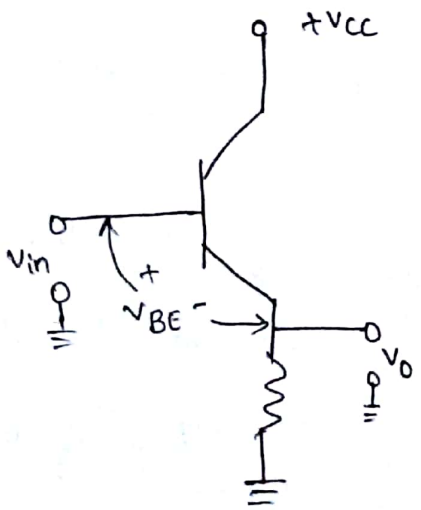
* Intermediate Stage is multi - stage Amplifier.

Level Shift Stage :

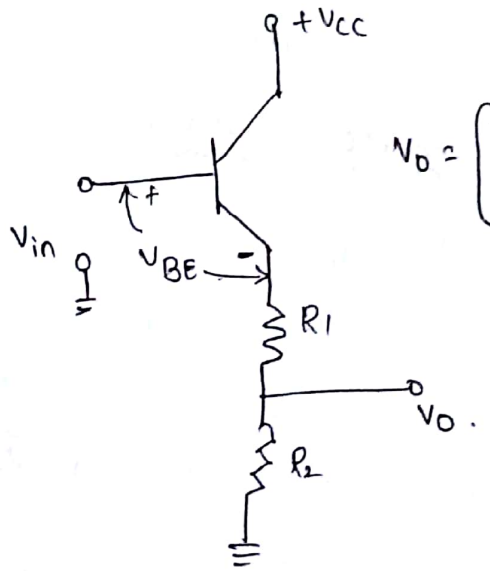
* The level shifter stage brings DC level to ground potential, when no signal is applied at i/p Terminals then Signal given to last stage which is o/p stage.

* The Buffer is usually, "Emitter follower", whose i/p impedance very high. This prevents loading Effect of high gain stage.

CKT 1 : Simple level shifting Ntwk :

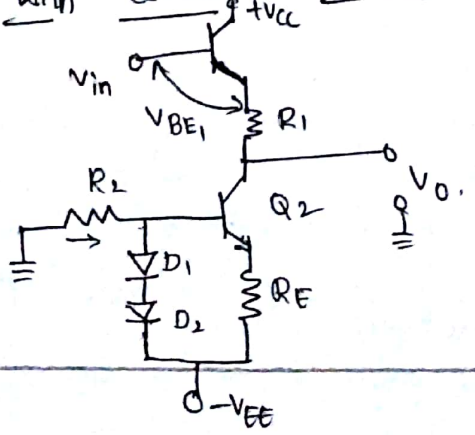


CKT 2 : Typical level shifting Ntwk



$$V_0 = \left[\frac{V_{in} - V_{BE}}{R_1 + R_2}\right] R_2$$

CKT 3 : Level Shifting With Constant Current Bias :



$$V_0 = V_{in} - V_{BE} - I_1 R_1$$

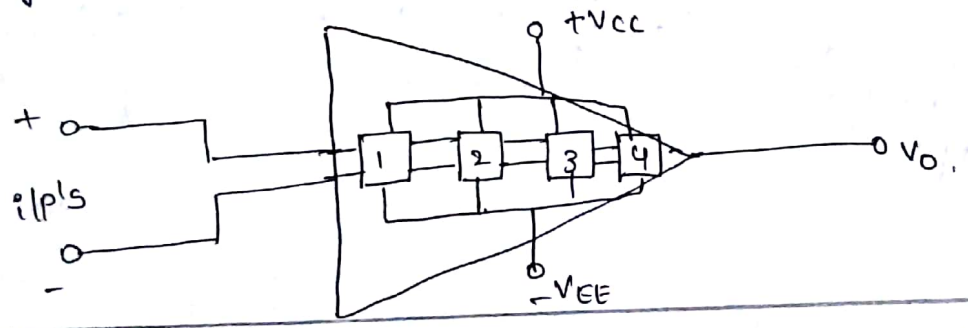
$$I_1 = I = \frac{V_{EE} - V_{BE}}{R_2}$$

Output Stage:

* The basic requirements of o/p stage

1. Large o/p vltg swing Capability
2. Large o/p Current Swing Capability.
3. Low o/p Impedance.
4. Low Quiscent power dissipation.
5. Short Circuit protection.

* All these Requirement satisfies push-pull Amplifier in class - AB (or) class - B. Hence commonly used in o/p stage of OP-Amp.



Ideal and Practical OP-Amp Specifications

Characteristics	Ideal	Practical
i/p OFF set Current [I_{IOS}]	0A	20nA.
I/P OFF set voltage [V_{IOS}]	0V	1mV.
Band Width (B)	∞	1MHz.
CMRR (ρ)	∞	90 dB.
Slew Rate (s)	∞	0.5 V/μsec
I/p bias Current (I_b)	0	80nA
PSRR	0	30μA/V.

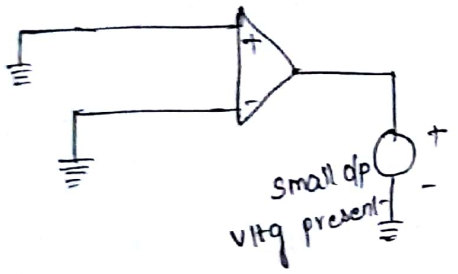
DC - characteristics of OP-Amp:

Output OFF-set voltage: The o/p OFF-set voltage is dc voltage present on the i/p Terminals when both i/p terminals are GND.

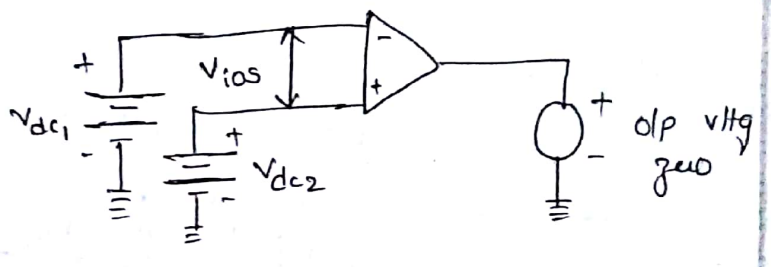
Both i/p OFF-set voltage and i/p bias current Contribute to generate o/p OFF-set voltage.

Input OFF Set voltage:

Case (i):



Case (ii):



* When both i/p Terminals of op-Amp are GND ideally, o/p vltg should be zero. But practically op-Amp shows small non-zero o/p vltg. This is due to mismatching present in internal CKT of an op-Amp.

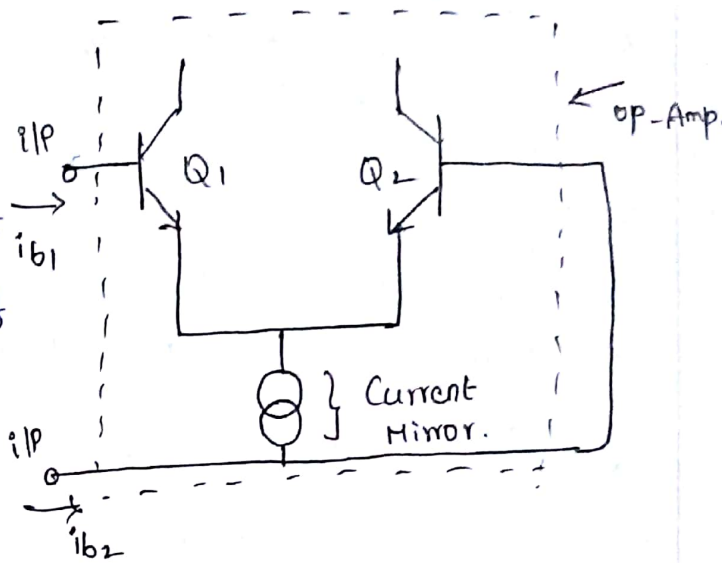
* Such vltg can cause an Error in practical application to make such voltage zero it is necessary to apply small difference vltg btw two i/p Terminals of op-Amp. This called S

Definition:

* The difference voltage must be applied between two i/p Terminals of an op-Amp to make o/p vltg zero. Called I/p OFF set voltage.

* It is denoted by V_{ios}.
* It depends on Temp, many Time one of i/p Terminals is applied with proper polarity. So as to Null o/p keeping other i/p Terminal GND.

Input OFF-Set Current:

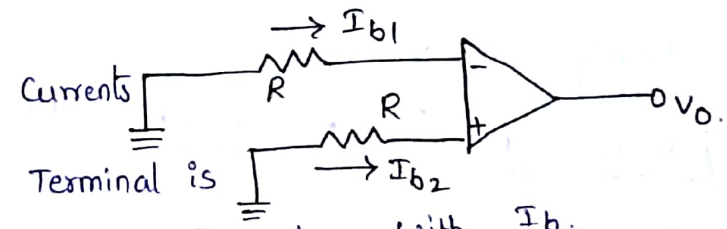


* The Algebraic difference between i/p Current following into 2 i/p Terminals of Op-Amp called I/p OFF set Current. & denoted by (I_{ios})

$$I_{ios} = |I_{b1} - I_{b2}|$$

→ Ideally (I_{ios}) = 0 ; practically : 200nA.

Input Bias Current:



* The Avg. value of two Currents following into Op-Amp i/p Terminal is called i/p bias Current and denoted with I_b.

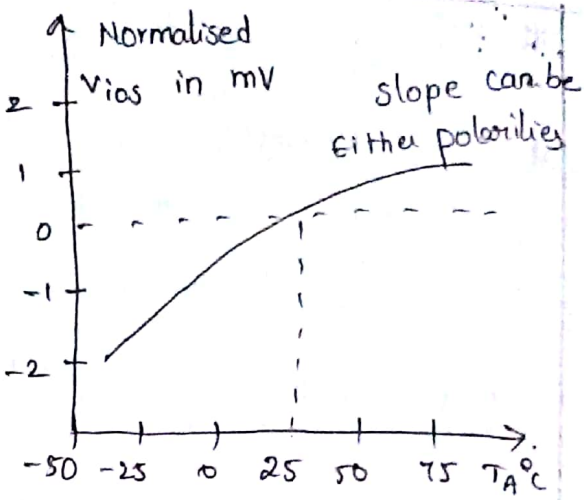
$$I_b = \frac{I_{b1} + I_{b2}}{2}.$$

Ideally $I_b = 0$; practically = 500nA.

Thermal Drift:

* Op-Amp parameters, i/p OFF-set vltg (I_b), (I_{ios}), are not Constant but vary with
  i) Temperature
  ii) Supply voltage changes
  iii) Time

Effect on V_{ios}:



* The Effect of change in Temp i/p OFF-Set voltage, defined by factor Called Thermal Voltage Drift
* It is also Called Input OFF-Set Voltage Drift.

Def:

It is defined as Avg. Rate of change of i/p OFF set voltage per unit change in Temp. and it is given by i/p OFF-set voltage Drift $= \frac{\Delta V_{ios}}{\Delta T}$

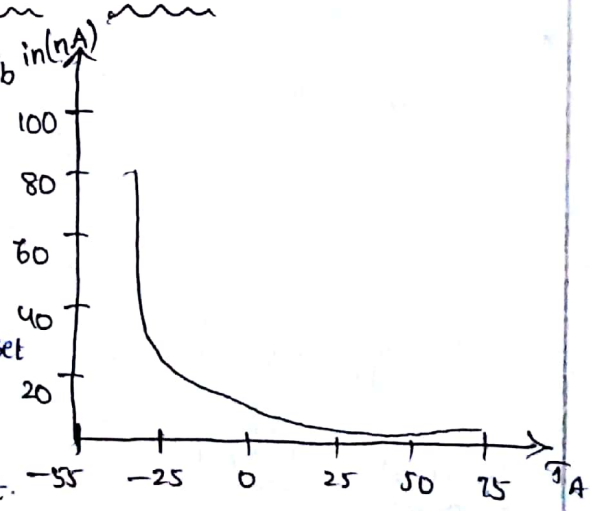
$\Delta V_{ios} \rightarrow$ change in i/p OFF-set voltage.

$\Delta T \rightarrow$ change in Temp.

UNITS : $\mu V / °c$.

Ideally at = 0 at 25°c

Effect on Input OFFset and Bias Current:



* The Effect of Temp on i/p I_b biased Current defined by factor Called i/p bias Current Drift.

Then

* The Effect of Temp on i/p offset Current is defined by factor is Called i/p OFF-Set Current Drift.

Def:-

The Avg. Rate of change of i/p bias Current per Unit change in Temp is called i/p bias Current Drift.

Thermal Drift in i/p bias Current $= \frac{\Delta I_b}{\Delta T} = \frac{nA}{^oC}$ (or) $\frac{PA}{^oC}$

Thermal Drift in i/p OFFset Current $= \frac{\Delta I_{ios}}{\Delta T}$

AC - characterstics of Op-Amp :

* The AC characterstics of OP-Amp 1. Slew Rate
2. Frequency Response.

Slew Rate :

* It indicates ability of Op-Amp with which it can change its o/p according to changes in i/p.

* It is defined as max. Rate of change of o/p v/tg. with Time is called slew Rate.

Units : v/μ-sec.

Slew Rate (s) : $\left.\frac{dv_o}{dt}\right|_{max}$.

* The slew Rate Caused due to limited changing Rate of compensatiting Capacitor and current limiting, saturation of internal stages of OP-Amp.

* When high freq. large Amp Signal applied when it given by $S = \frac{dV_c}{dt} = I/c$

* for large charging Rate, Capacitor should be small charging Current should be large. Hence slew Rate for an OP-Amp whose max. internal Capacitor charging Current is known then slew rate given by

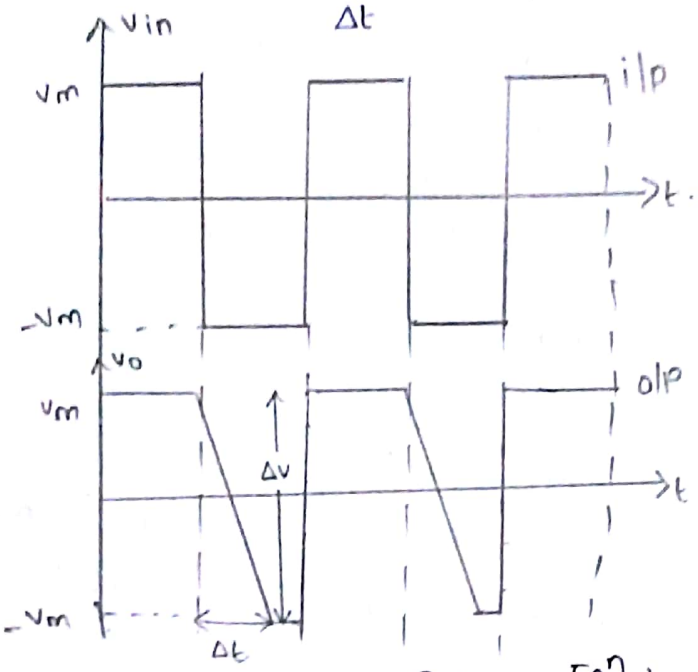
$$S = \frac{I_{max}}{C}.$$

Effect of Slew Rate :

Consider CKT using op-Amp having Unit gain. If i/p is square wave, o/p has to be square wave but this observed for certain freq of i/p due to slew rate of op-Amp a particular i/p freq. o/p get distorted

It given by slew Rate as

$$S = \frac{\Delta V_o}{\Delta t} \quad V/sec.$$



Calculation of Slew Rate Eqn :

Gain of op-Amp is Unity with purely sine i/p and o/p must be same as i/p

$$V_s = V_m \sin\omega t$$

$$V_o = V_m \sin\omega t.$$

$$S = \frac{dV_o}{dt} = V_m\left[\cos\omega t\,(\omega)\right] = V_m\,\omega\,\cos\omega t.$$

$$S = \left.\frac{dV_o}{dt}\right|_{max} = S = V_m(\omega) \quad (\because \max \cos\omega t = 1).$$

$$= 2\pi f_m V_m \Rightarrow \boxed{f_m = \frac{S}{2\pi V_m}}$$

Frequency Response of OP-Amp:

* For Ideal OP-Amp, infinite BW. that makes gain of op-Amp must reminds a for all frequency from zero to infinite.

* But gain of practical op-Amp as Constant that mean gain decreases at higher [practical]. Such a gain Reduction w.r.t freq. is called Roll off.

* Mathematically, It is complex number, and its magnitude and phase Angle changes with frequency.

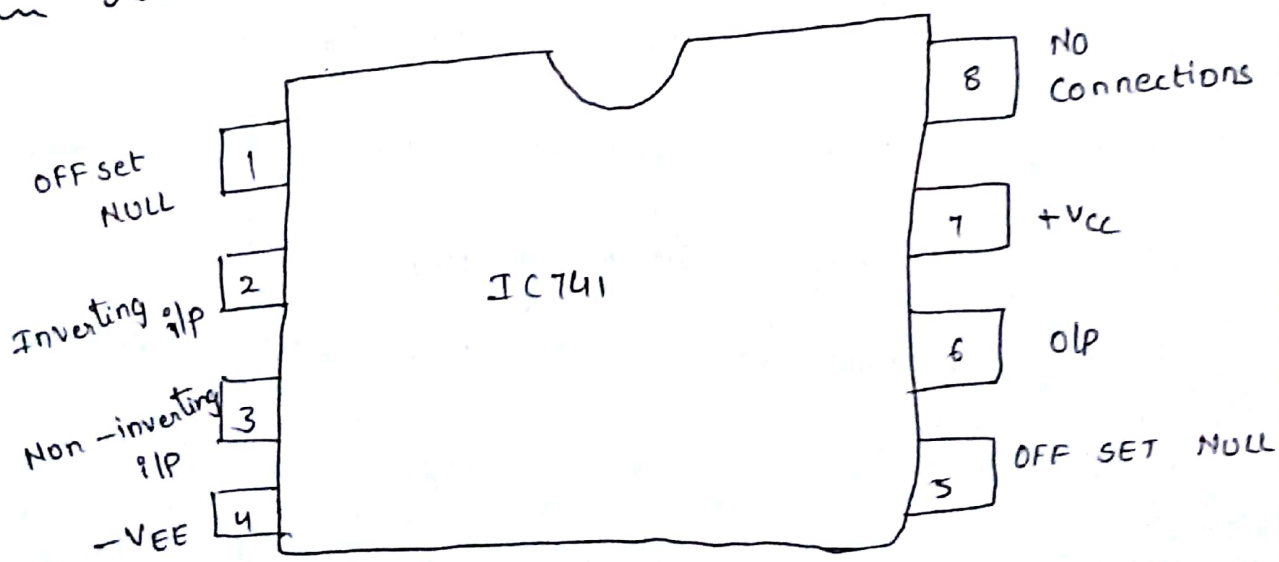
Bode - plot:

The plot drawn in between phase Angle Vs freq is called Bode plot.

Magnitude Plot:

The plot drawn in between Gain Vs freq is called so.

741 - OPAMP:



8 - pin Diagram

Ideal Vs Practical characteristics of IC741 OP-Amp.

S.NO	Parameters	Symbol	Ideal	Practical
1.	Open loop voltage Gain	A_{OL}	∞	2×10^5
2.	Output Impedance	Z_{out}	0	75 Ω
3.	Input Impedance	Z_{in}	∞	2 MΩ
4.	I/p OFF-set Current	I_{ios}	0	20 nA.
5.	I/p OFF-set Voltage	V_{ios}	0	1mV.
6.	Band Width	BW	∞	1 MHz
7.	CMRR	ρ	∞	90 dB.
8	Slew Rate	S	∞	0.5 V/μ-sec
9.	I/p bias Current	I_b	0	80 nA.
10.	PSRR	PSRR	0	30μV/V.

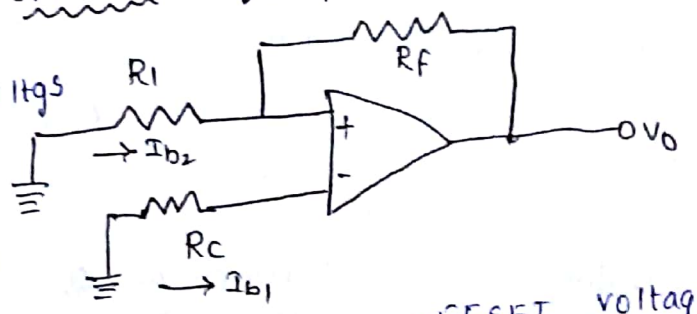
Classes of OP-Amp IC741 :

class	Type	Remark.
741	Millitary Grade	Temp. Range [−55°c to +125°c]
741 A	Improve version of 741	Better Electrical characteristics
741 C	Commercial Grade	Temp Range [0°c to 70°c]
741 E	Improved version of 741C	Better Electrical characterstics
741 S	Millitary Grade	Higher slew Rate.
741 SC	Commercial Grade	Higher slew Rate.

Features of IC741 - OPAMP :

1. No frequency compensation Required
2. Short CKT protection provided.
3. OFF-set vltg NULL capability.
4. Large common Mode and Differential voltage Range.
5. No - Latch up.

Measurement of O/p OFF-SET voltage :



It is diff. btw DC vltgs present at when both i/p Terminals are GND

It is due to i/p OFFset voltage OFFSET voltage & also due to i/p bias current. Denoted by (V_{oos})

$$V_{o1} = I_{b2} \cdot R_1 \left(\frac{R_f}{R_1}\right) \quad \text{--- (1)}$$

$$V_{o2} = I_{b1} \; R_c \left(1 + \frac{R_f}{R_1}\right) \quad \text{--- (2)}$$

practically R_c value similarly equal to R_1

$$V_{o2} = I_{b1} \; R_1 \left(\frac{R_1 + R_f}{R_1}\right) = I_{b1}(R_1 + R_f)$$

$$V_{o1} + V_{o2} = -I_{b2} R_f + I_{b1} R_1 + I_{b1} R_f$$

$$= R_f (I_{b1} - I_{b2}) + I_{b1} R_1$$

$$= R_f (I_{ios}) + I_{b1} R_1$$

The o/p vltg, due to i/p offset vltg is given by :

$$V_{ios}\left[1+R_f/R_1\right] \quad \text{--- (4)}$$

Hencence total OFFSET vltg is given by

$$V_{oos} = V_{ios}\left(1+\frac{R_f}{R_1}\right) + R_f\,(I_{ios})$$

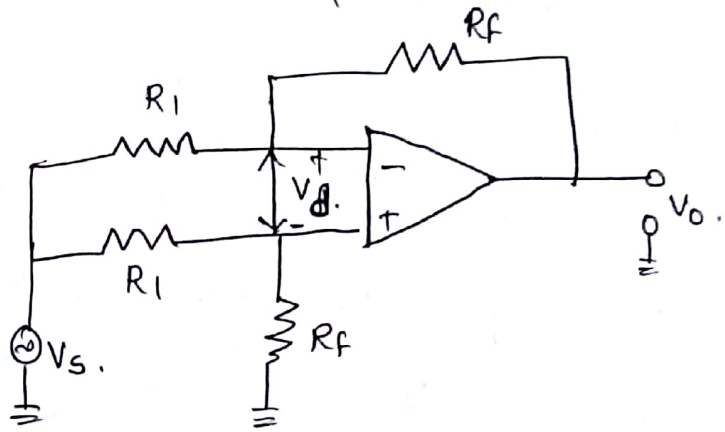
Measurement of PSRR :

It is Ratio of chang in i/p OFFSet vltg to change in supply voltage (V_{cc}).

$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{cc}}$$

Derivation & Measurement of CMRR :

The Ratio of [Ad] to Common Mode Gain (Ac) Mathematically, expressed as $(\rho) = \left|\frac{A_d}{A_c}\right|$.



Derivation :

The common mode slg V_s applied to both i/p's Thus at point A and B common Mode slg vltg is V_c. Then

$$V_B = \text{Vltg at point } B = \frac{V_s \cdot R_f}{R_1+R_f}.$$

$$\text{Grounding } (V_o),\quad V_{A_1} = \frac{V_s \cdot R_f}{R_1+R_f}$$

$$\text{Grounding } (R_1),\quad V_{A_2} = V_o\, R_1 / R_1+R_f$$

$$\text{common Mode } (A_c) = \frac{V_o}{V_c} = \frac{V_o}{V_s}.$$

$$V_A = \frac{V_o R_1 + V_s R_f}{R_1 + R_f}$$

$$V_d = V_B - V_A$$

$$V_d = \frac{V_s R_f - V_o R_1 - V_s R_f}{R_1 + R_f} = \frac{-V_o R_1}{R_1 + R_f}$$

$$A_d = \frac{-(R_1 + R_f)}{R_1}.$$

$CMRR = \left|\frac{A_d}{A_c}\right|$ = Hence CMRR can be Measured.

Frequency Compensation Technique:

If stable op-Amp CKT has single break corner frequency but it has three break (or) corner frequency due to Capacitive Component produces by various no of stages Then open loop frequency dependent T/F of Such system Can Assumed as

$$A_{OL}(f) = \frac{A_{OL}\ (\text{at } f=0)}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)} \qquad 0 < f_1 < f_2 < f_3.$$

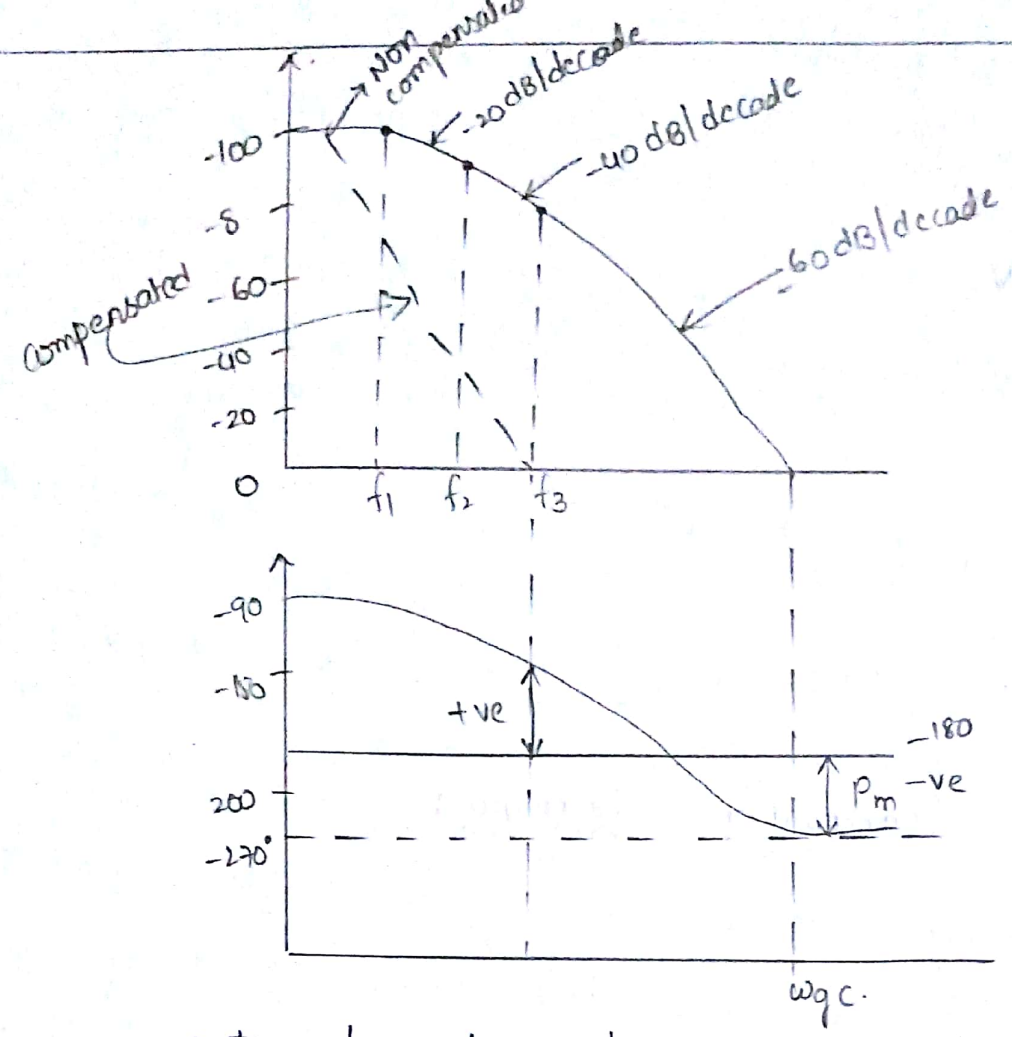
Laplace domain it can be expressed as

$$A_{OL}(s) = \frac{A_{OL}}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$

The phase shift Such loop Gain

$$\phi(f) = -\tan^{-1}(f/f_1) - \tan^{-1}(f/f_2) - \tan^{-1}(f/f_3)$$

$$= -\phi_1 - \phi_2 - \phi_3.$$



* For system has closed loop gain and is required. Choose suitable Compensation Technique

* There are two Types of Compensation Techniques.

  i) External Compensation

  ii) Internal Compensation.

* In External Compensation Technique.

  i) Dominant pole

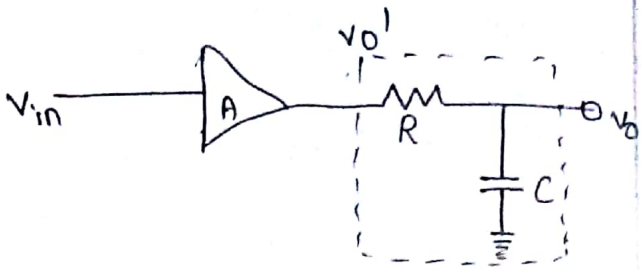
  ii) Pole - zero

  iii) feed forward.

<u>Dominant - pole</u>:

Dominant pole introduced by adding Compensating Ntwk i.e., RC NtWK, This means pole with mag & much Smaller than existing poles and break freq of compen

$$A_1 = \frac{V_o}{V_o'}$$



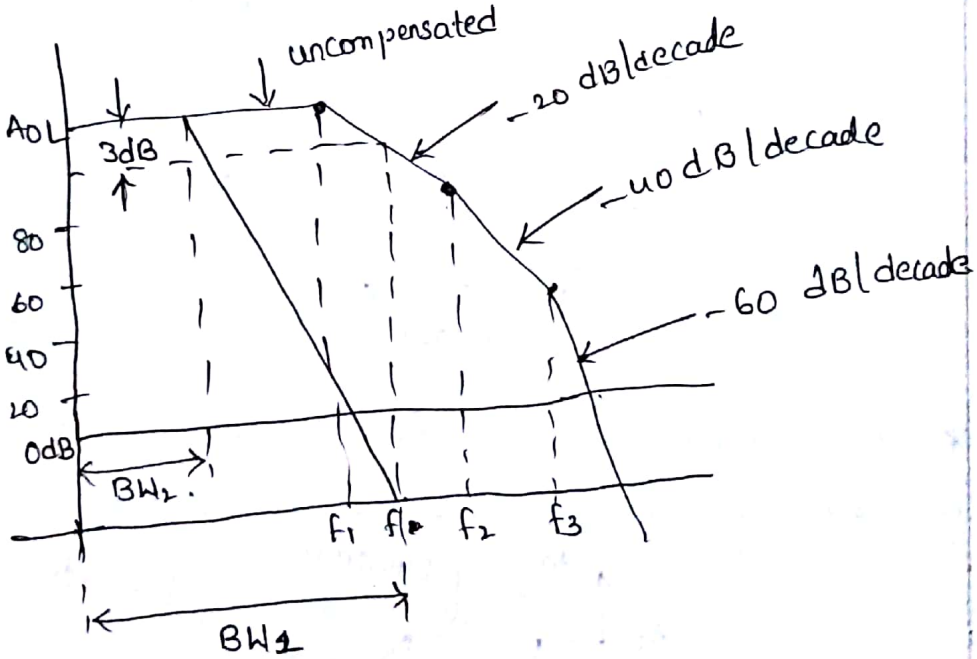
$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_C}{R - jX_C}$$

$$= \frac{-j/2\pi f_c}{R - j/2\pi f_c}$$

$$f_d = \frac{1}{2\pi RC} \qquad A_1 = \frac{1}{1+j(f/f_d)}$$

$$A' = A A_1$$

$$\bar{A} = \frac{A_{OL}}{1+j(f/f_d)(1+jf/f_1)\left(1+j\frac{f}{f_2}\right)(1+j\,f/f_3)}$$



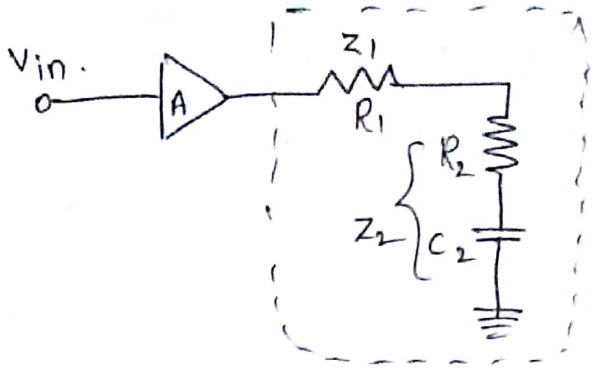
Pole - Zero Compensation :

Consider same op-Amp described by openloop (A)

$$A = \frac{A_{OL}}{(1+j\,f/f_1)(1+j\,f/f_2)(1+j\,f/f_3)}$$

T/F is $A_1 = \frac{V_o}{V_i}$

By vltg divide Rule.



$$A_1 = \frac{Z_2}{Z_1 + Z_2}$$

$Z_2 = R_2 - jX_{C_2}$ $\quad Z_1 = R_1$

$$A_1 = \frac{R_2 - jX_{C_2}}{R_1 + R_2 - jX_{C_2}} = \frac{R_2 + 1/j2\pi f C_2}{R_1 + R_2 + 1/j2\pi f C_2}$$

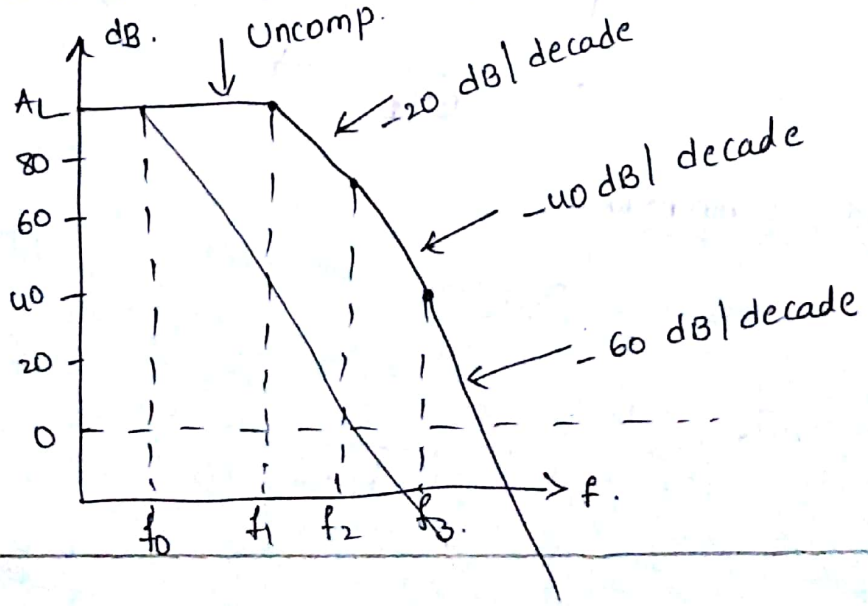
$$f_1 = \frac{1}{2\pi R_2 C_2} \qquad f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$$

$$A = \frac{1 + j(f/f_1)}{1 + j(f/f_0)}.$$

$$A' = AA_1$$

$$= \frac{A_{OL}\,(1 + j(f/f_1))}{(1 + j(f/f_0))(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)}$$

* The first corner frequency (f_0) gain is -20 dB/decade at f_0.
In this compensation BW is improved Equal to $(f_2 - f_1)$



Internal Compensation Technique :

* OP-Amp like IC741 compensation provided internally, which generally built in log compensation.

* A capacitor ranging from 10 to 30 PF is fabricated btw i/p & o/p stage to achieve necessary compensation.

* This type of compensation called Miller - Effect Compensation such OP-Amp called Compensated OP-Amps.

UNIT - III

INTRODUCTION:

* The op-Amp is generally used in closed loop configuration using Feedback.
* Applications of op-Amp are classified into 2 types
  - i) Linear Applications
  - ii) Non-linear Applications

Linear Applications:

* In Linear Application o/p Vltg varies linearly w.r.t to the i/p Vltg.
* The Negative F/B used from amplifier o/p to inverting i/p Terminal.
* Some Applications
  1. Voltage follower
  2. Adder, subtractor
  3. Instrumentation Amplifier.
  4. Integration & Differentiator etc.

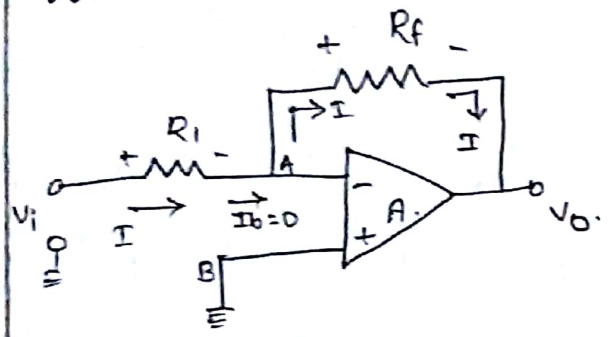
Non-Linear Application.

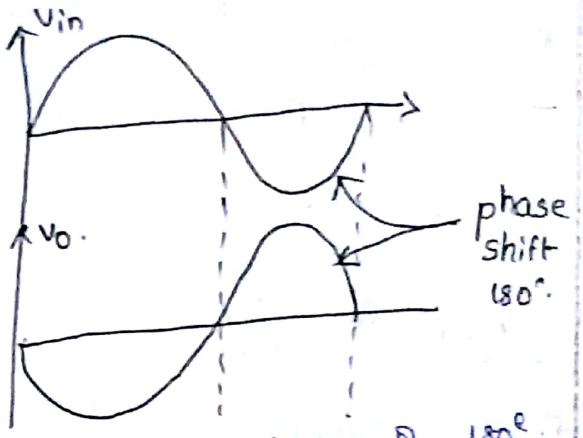
* The F/B is provided from o/p to Non-inverting i/p Terminal.
* The F/B may be provided to inverting i/p Terminal using Non-linear Elements like Diodes, Trans. etc.
* Non-linear CKTs have highly non-linear i/p to o/p characteristics.

Applications:

1. Precision Rectifiers
2. Log Amplifiers
3. Anti-log Amplifiers
4. Comparators
5. Schmitt Trigger. etc

Ideal Inverting Amplifier:





Def: An Amplifier which provide phase shift of 180° btw i/p and o/p is called Inverting Amplifier.

Derivation of closed Loop:

If Node B is GND, Node 'A' is also ground potential. So $V_A = 0$ $\quad I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1}$

Current Direction (I) is from o/p side considering

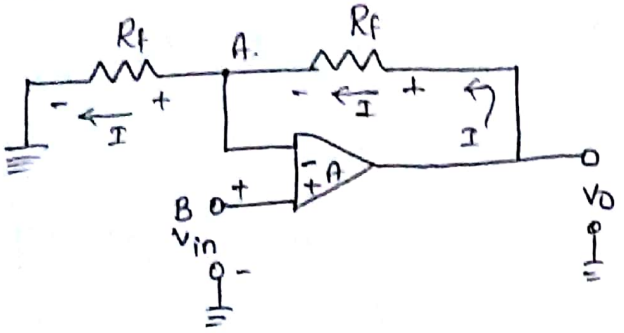
$$I = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$$

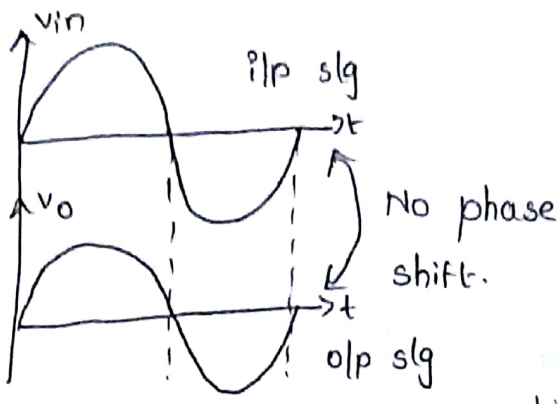
$$\frac{V_{in}}{R_1} = \frac{-V_o}{R_f}.$$

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1} = A_{vf}$$

* : A_{vf} is known as Gain with F/B. The Negative sign indicates polarities of o/p is opposite to that i/p Hence it is also known as Inverting Amp.

Ideal Non-Inverting Amplifier :





Def: An Amplifier which does not provides phase shift of 180° between i/p and o/p called Non-Inverting Amp.

The Node B is at potential V_{in}, Hence potential of "A" is same as B, which is V_{in} (from virtual GND)

$$V_{in} = V_A = V_B.$$

From o/p side, we can write ; $I = \frac{V_o - V_A}{R_f} = \frac{V_o - V_{in}}{R_f}$ —— ①

At inverting Terminal $(I) = \frac{V_A - 0}{R_1} = \frac{V_{in}}{R_1}$ —— ②

① = ②

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

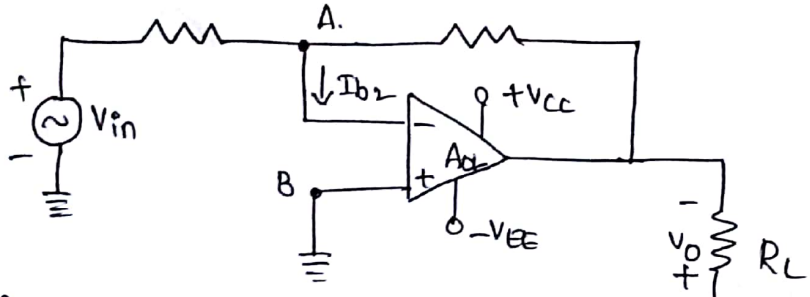
$$\frac{V_o}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$$

$$\boxed{\frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}} = A_{vf}.$$

COMPARISION IDEAL & NON-IDEAL INVERTING AMP.

S.NO	Ideal Inverting Amp	Ideal Non-Inverting Amp.
1.	Voltage Gain = $-R_f/R_1$	Voltage Gain = $1+R_f/R_1$
2.	The o/p is inverted w.r.t to i/p	No phase shift b/w i/p and o/p
3.	Voltage Gain Can adjusted as greater than, Equal, ≤ 1	Vltg gain always > 1.
4.	The i/p impedance is R_1	I/p impedance extremely large.

Practical Inverting Amplifier:



Main Difference of Ideal Vs practical:

1. The i/p Resistance (R_{in}) less than infinity Hence OP-Amp i/p current is finite.
2. Its open loop voltage Gain less than infinity
3. Its o/p Resistance (R_o) is not zero.

Derivation Closed Loop Voltage Gain:

Apply KCL at node "A".

$$I_{in} = I_f + I_{b2}$$

We know that R_{in} is not "∞" but it very large hence I_{b2} is negligible small & it be neglected

$I_{in} = I_f$.

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_o}{R_f} \quad \text{——— (1)}$$

From Eq. CKT of op-Amp $V_o = A_{OL} \cdot V_d$.

$$= A_{OL}(V_1 - V_2)$$

$V_1 = 0 \quad V_2 = V_A$.

$$V_o = A_{OL}(-V_A) \quad \text{——— (2)}$$

Sub V_o in Eq^n (1).

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A + A_{OL} V_A}{R_f}$$

$$\frac{V_{in} + V_o/A_{OL}}{R_1} = \frac{-V_o}{A_{OL}} \quad -V_o/R_f$$

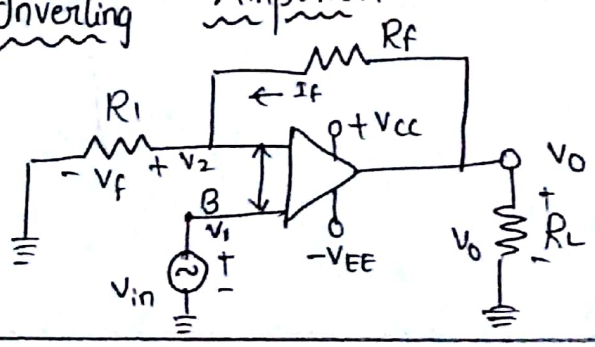
$$V_{in} R_f + \frac{V_o R_f}{A_{OL}} = \frac{-V_o R_1}{A_{OL}} \quad -V_o R_1$$

$$V_{in} R_f = -\left[\frac{V_o R_f}{A_{OL}} \left(\frac{V_o R_1}{A_{OL}} + V_o R_1\right)\right]$$

$$= -V_o \left[\frac{R_f}{A_{OL}} + R_1 + \frac{R_1}{A_{OL}}\right]$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{-R_f \cdot (A_{OL})}{R_f + R_1 A_{OL} + R_1} = A_{CL}}$$

Practical Non-Inverting Amplifier:



Derivation of closed Loop Voltage Gain:

W.K.T $V_o = A_{OL} \cdot V_d$

$$= A_{OL}(V_{o1} - V_{o2})$$

$$= A_{OL}(V_{in} - V_f)$$

Using vltg divider Rule

$$V_f = \left(\frac{V_o}{R_1 + R_f}\right) R_1$$

$$V_o = A_{OL}\left[V_{in} - \frac{V_o R_1}{R_1 + R_f}\right]$$

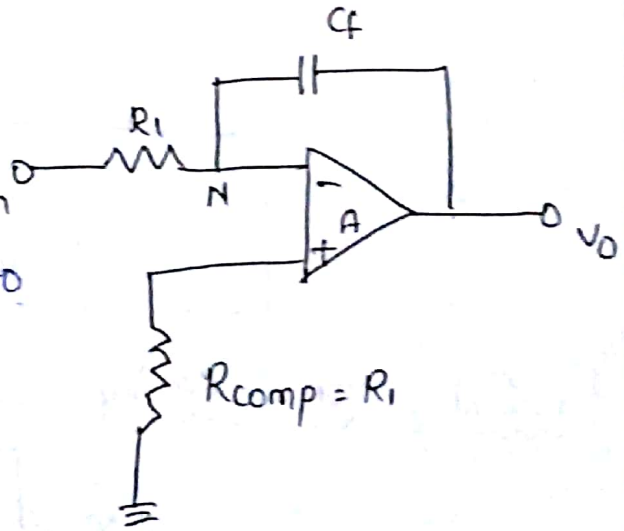
$$= A_{OL} V_{in} - \frac{A_{OL} V_o R_1}{R_1 + R_f}$$

$$V_o + \frac{A_{OL} V_o R_1}{R_1 + R_f} = A_{OL} V_{in}$$

$$\frac{V_o}{V_{in}} = \frac{A_{OL}(R_1 + R_f)}{R_1 + A_{OL} R_1 + R_f}$$

Integrator:

The CKT provides an o/p V_{in} voltage which proportional to Time integral of i/p and $R_1 C_f$ is Time Constant of Integrator



Proof :

At Node (N) Apply KCL $\frac{V_i}{R_1} + C_f \frac{dv_o}{dt} = 0$

$$C_f \frac{dv_o}{dt} = -\frac{V_i}{R_1}$$

$$V_o = \frac{-1}{R_1 C_f} \int V_i \, dt.$$

The Negative sign indicates F/B is connected Negative Terminal of Op-Amp.

This Integrator is known as Inverting Integrator

Take Laplace Transform. on both sides to o/p Eq^n.

$$V_o(s) = \frac{-1}{R_1 C_f s} V_i(s)$$

In steady state $s = j\omega$.

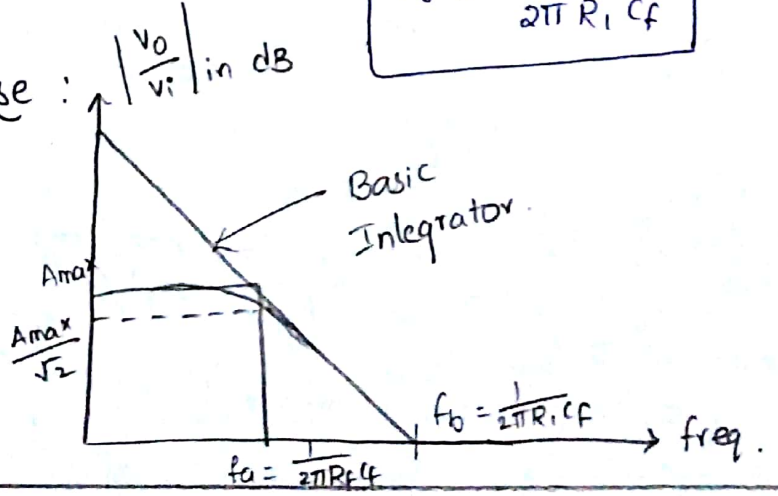
$$V_o(j\omega) = \frac{-1}{R_1 C_f j\omega} V_i(j\omega)$$

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|\frac{-1}{jR_1 C_f \omega}\right| = \frac{1}{\omega R_1 C_f}$$

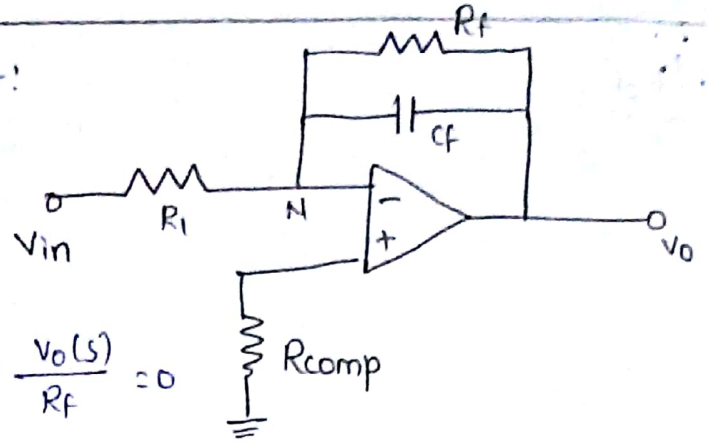
Then frequency of Integrator is $\frac{1}{2\pi f R_1 C_f} = |A|$.

$$\boxed{f_b = \frac{1}{2\pi R_1 C_f}}$$

frequency Response :



Practical Integrator Circuit:



At Node (N), Apply KCL

usin L.T.

$$\frac{V_i(s)}{R_1} + s \cdot C_f \cdot V_o(s) + \frac{V_o(s)}{R_f} = 0$$

$$V_o(s)\left[s C_f + \frac{1}{R_f}\right] = \frac{-V_i(s)}{R_1}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-1}{R_1\left(sC_f + 1/R_f\right)}$$

$$= \frac{-R_f}{R_1 s C_f + R_1}$$

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|\frac{-1}{j\omega C_f R_1 + \frac{R_1}{R_f}}\right|$$

$$|A| = \left[\frac{1}{\omega^2 C_f^2 R_1^2 + (R_1/R_f)^2}\right]^{1/2}.$$

$$= \frac{\left(\frac{R_f}{R_1}\right)}{\sqrt{1+\omega^2 C_f^2 R_f^2}}$$

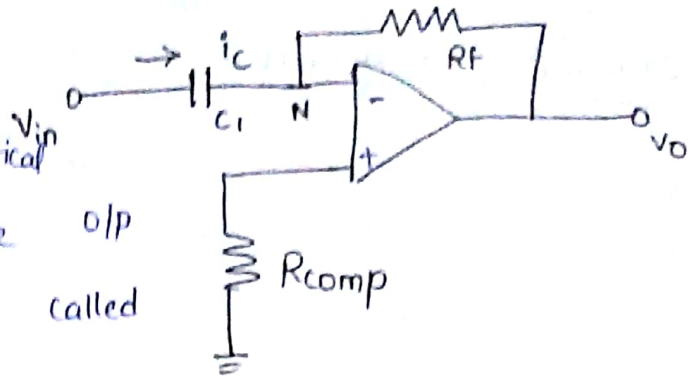
$$|A| = \frac{1}{\sqrt{2}}$$

$$\frac{1}{\sqrt{2}} = \frac{(R_f/R_1)}{\sqrt{1+\omega^2 C_f^2 R_f^2}}$$

$$\sqrt{2} = \sqrt{1+\omega^2 C_f^2 R_f^2}$$

$$\omega C_f R_f = 1 \Rightarrow \boxed{f = \frac{1}{2\pi C_f R_f}}$$

Differentiator:



The CKT performs mathematical operation, differentiator the o/p is derivative of i/p is called Differentiator.

"N" $\rightarrow V_N = 0$

The Current through capacitor $I_c = C_1 \frac{d}{dt}(V_i - V_N)$

$= C_1 \frac{dV_i}{dt}$

Apply KCL at Node (N)

$$C_1 \frac{dV_i}{dt} + \frac{V_o}{R_f} = 0$$

$$\frac{V_o}{R_f} = -C_1 \frac{dV_i}{dt}$$

$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

$$V_o = -R_f C_1 \frac{d}{dt}(V_i)$$

The Eqn says that o/p is derivative of i/p

Apply L.T on 2 sides.

$$V_o(s) = -R_f C_1 s \cdot (V_i(s))$$

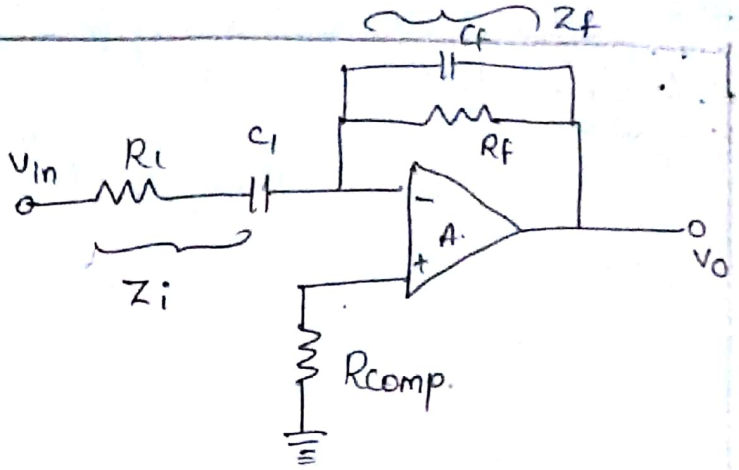
$$\frac{V_o(j\omega)}{V_i(j\omega)} = -R_f C_1 (j\omega)$$

$$|A| = |-j\omega R_f C_1| = \omega R_f C_1$$

$$\Rightarrow |A| = 1 \Rightarrow 2\pi f_a R_f C_1 = 1$$

$$\boxed{f_a = \frac{1}{2\pi R_f C_1}}$$

Practical Differentiator:



T/F of CKT is

$$\frac{V_o(s)}{V_i(s)} = \frac{-Z_f}{Z_i}$$

$$= \frac{sR_f C_1}{(1+sR_f C_f)(1+sR_1 C_1)}$$

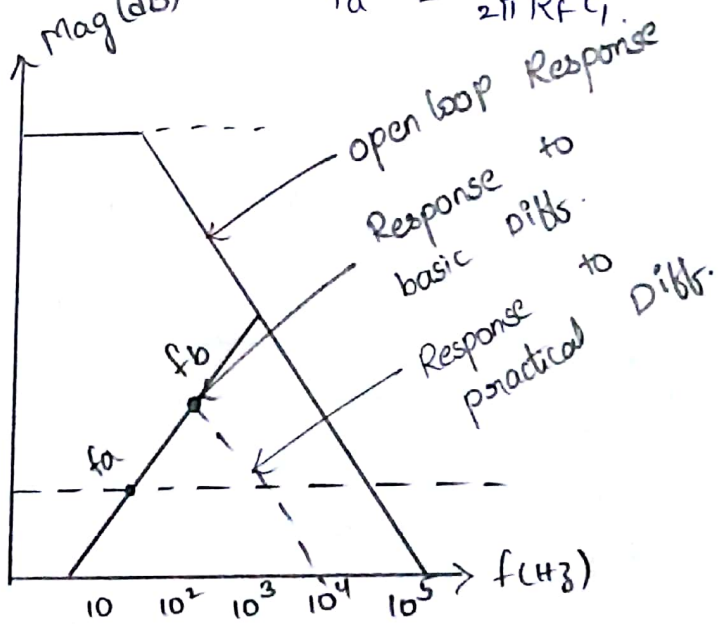
from CKT $R_f C_f = R_1 C_1$

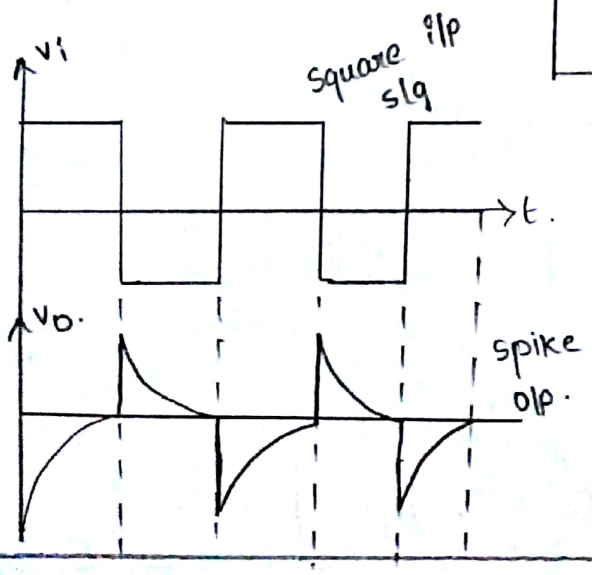
$$\frac{V_o(s)}{V_i(s)} = \frac{sR_f C_1}{(1+sR_f C_1)^2}$$

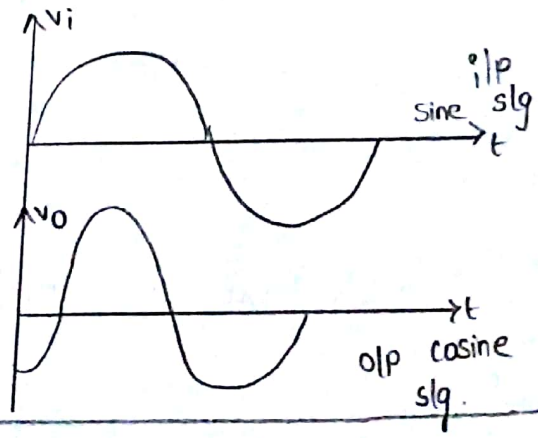
from this T/F practical freq. $f_b = \frac{1}{2\pi R_1 C_1}$

$f_a = \frac{1}{2\pi R_f C_1}$

frequency Responsence:







Instrumentation Amplifier:

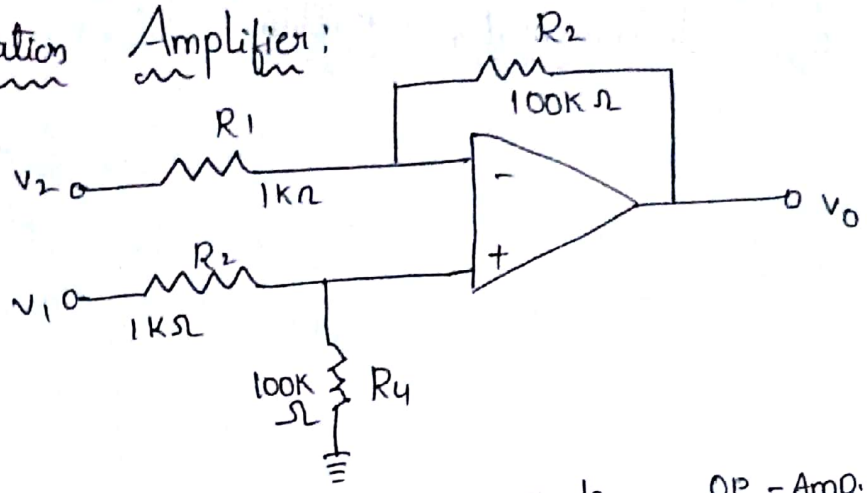


Fig (a): Diff. Amp using single op-Amp.

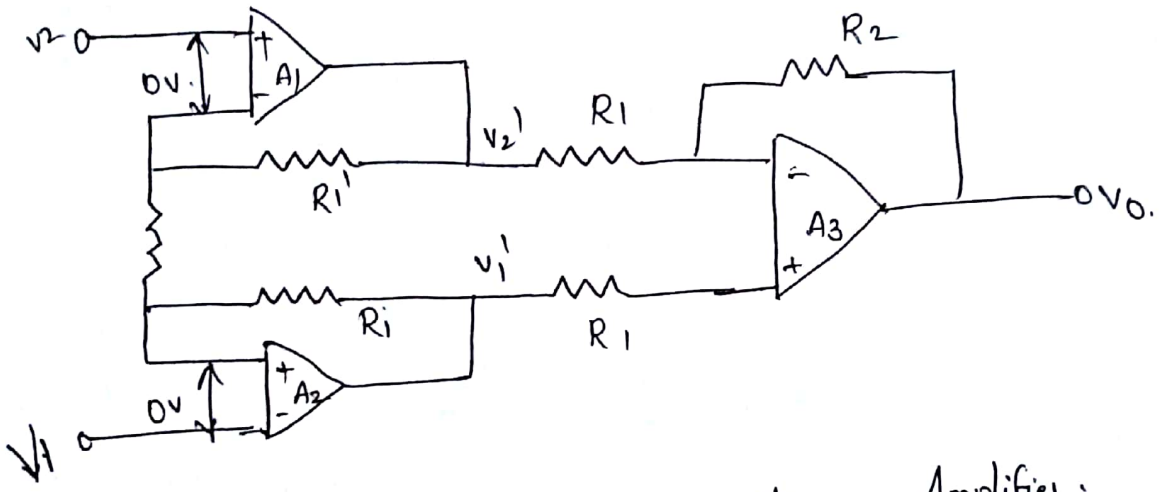


Fig: (b): Improved Instrumentation Amplifier.

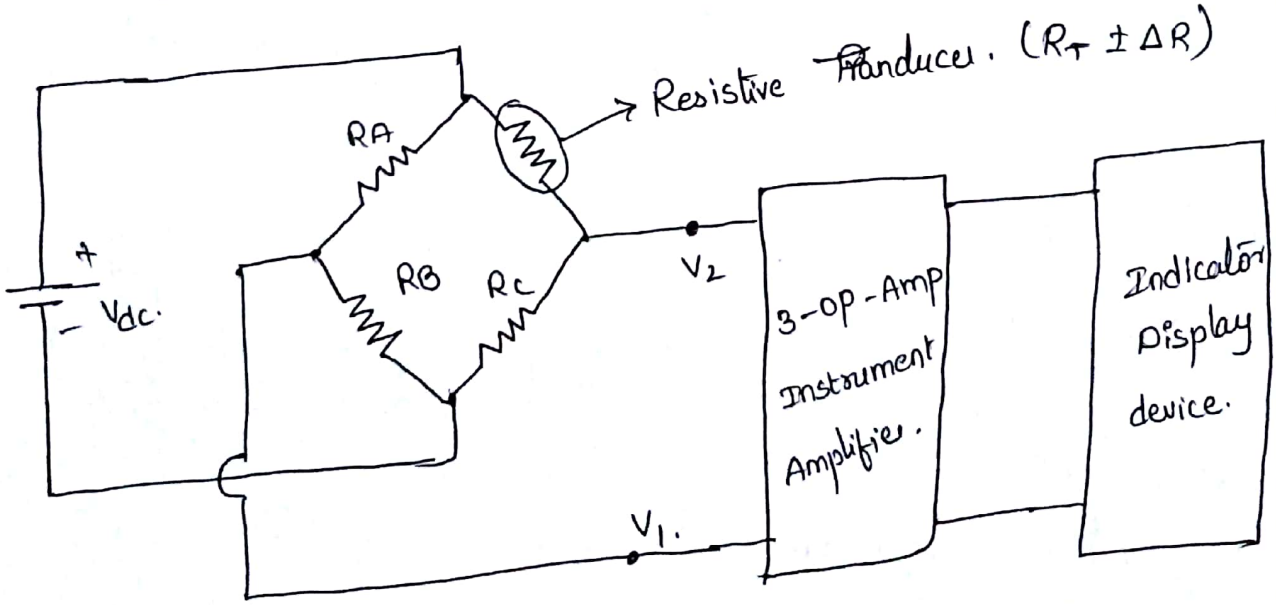


Fig (c): Instrumentation Amplifier using Transducer.

Features of Instrumentation Amplifier:

1. High Gain Accuracy
2. High CMRR
3. High Gain stability with low Temp coefficient.
4. Low DC OFF-SET
5. Low o/p impedance.

The o/p of Diff. Amp is

$$V_0 = \frac{-R_2}{R_1} V_2 + \frac{1}{1+\frac{R_3}{R_4}} (V_1) \left[1 + \frac{R_2}{R_1}\right]$$

Take common $-R_2/R_1$

$$V_0 = \frac{-R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}} V_1 \left(1+\frac{R_2}{R_1}\right)\right]$$

But $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ then o/p given by:

$$V_0 = -\frac{R_2}{R_1}(V_2 - V_1) = \frac{R_2}{R_1}(V_1 - V_2)$$

For fig (b):

The o/p of instrumentation Amp given by

$$V_0 = -\frac{R_2}{R_1} V_2' + \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2 V_2'}{R_1+R_2}\right).$$

Take Common $\frac{R_2}{R_1}$

$$V_0 = \frac{R_2}{R_1}(V_1' - V_2')$$

$$V_1' = R'I + V_1 \qquad V_2' = -R'I + V_2.$$

The (I) Having through (R) and given by

$$I = \frac{V_1 - V_2}{R}.$$

Sub V_1' and V_2' in V_0 Eq^n.

$$V_0 = \frac{R_2}{R_1}\left[R'I + V_1 + R'I - V_2\right]$$

$$= \frac{R_2}{R_1}\left[2R'I + V_1 - V_2\right]$$

$$= \frac{R_2}{R_1}\left[\frac{2R'}{R}\left[(V_1 - V_2) + V_1 - V_2\right]\right].$$

$$= \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

$$= V_1 - V_2\left[\frac{R_2}{R_1}\cdot\left(\frac{2R'}{R} + 1\right)\right].$$

AC Amplifier :

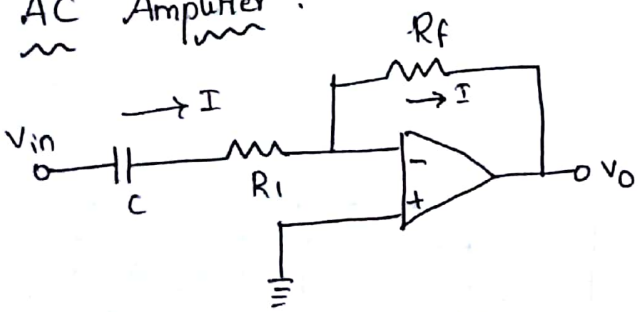
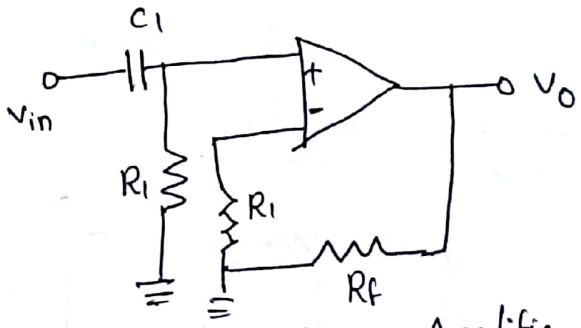


Fig (a) : Inverting Amplifier.



b) Non - Inverting Amplifier

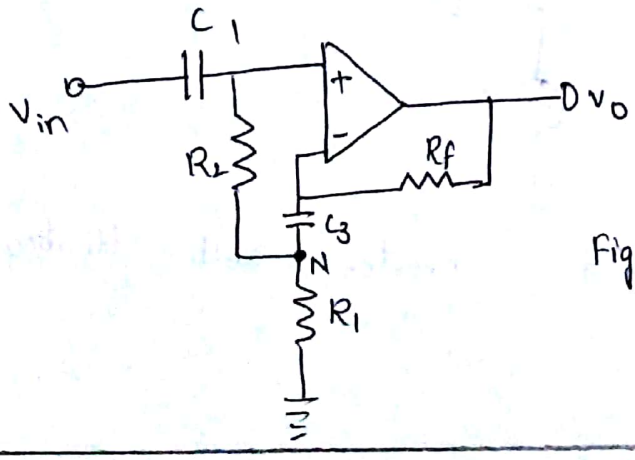


Fig c) : High i/p impedance of Non - Inverting AC - Amp

The o/p v/tg of Inverting AC Amp given by

$$V_o = -R_f I.$$

Where $I = \dfrac{V_i}{R_1 + \frac{1}{sC}}$

$$V_o = \frac{-R_f V_i}{R_1 + 1/sC}$$

Gain of AC Amplifier $A_{CL} = \left|\dfrac{V_o}{V_i}\right| = \dfrac{-R_f}{R_1 + 1/sC}.$

Take Common R_1

$$A_{CL} = \frac{-R_f}{R_1}\left[\frac{1}{1+\frac{1}{R_1 sC}}\right] = \frac{-R_f}{R}\left[\frac{s}{s+\frac{1}{R_1 C}}\right]$$

from above Eq^n, freq given by $f_L = \dfrac{1}{2\pi R_1 C}$. At mid freq, capacitor acts as short CKT, then gain becomes $\boxed{-\dfrac{R_f}{R_1} \simeq A_{CL}}$

V to I Converter:

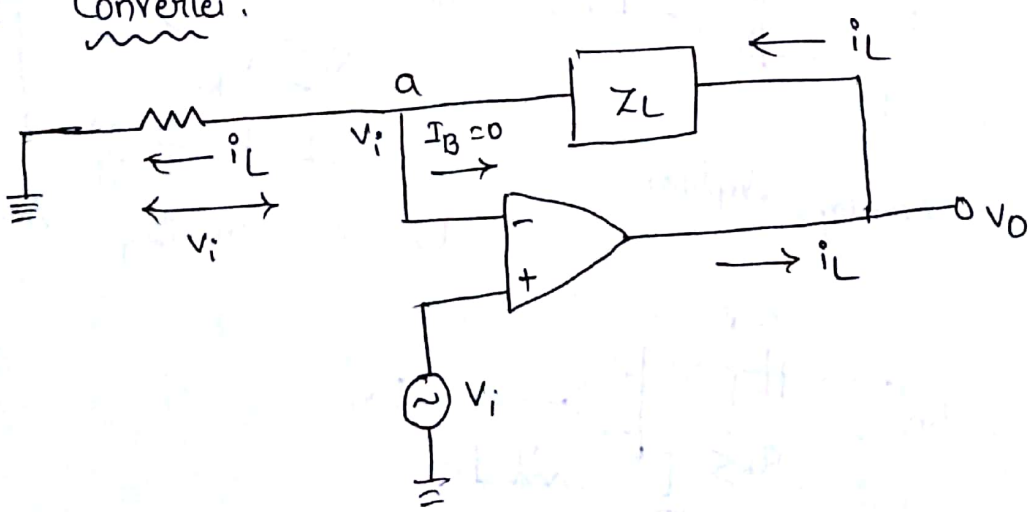


Fig: (a) : V to I Converter with floating Load.

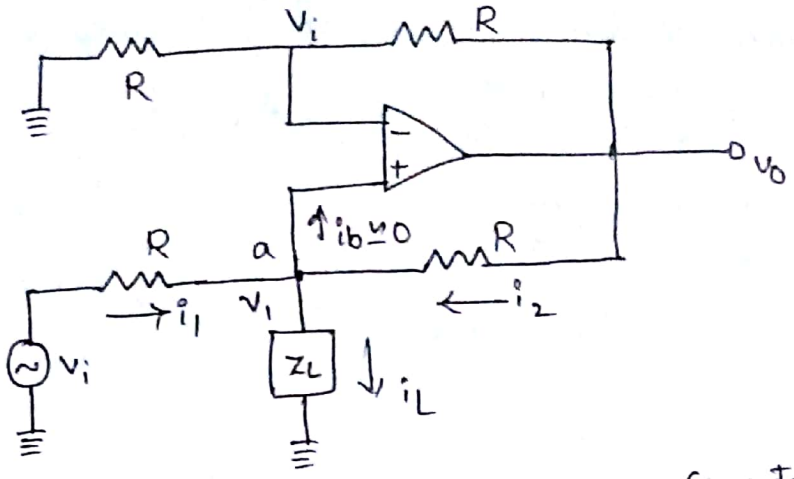


Fig (b): Voltage to Current Converter with GND load

Definition:

* The CKT to convert a voltage signal to proportional o/p current called V to I converter.
* There are two Types 1. V to I with floating load
  2. V to I with Grounded load

V to I Converter with Floating Load:

In this CKT load (Z_L) floating then vltg at (A) is here.

$$V_i = I_L R_1 \Rightarrow \boxed{I_L = \frac{V_i}{R_1}}$$

V to I Converter with Grounded Load:

Let V_1 be vltg at node (a). Apply KCL at (a)

$$i_1 + i_2 = i_L$$

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R.$$

$$V_1 = \frac{V_i + V_o - i_L R}{2}$$

The OP-Amp used in Non-Inverting mode. The gain of CKT $1 + \frac{R}{R} = 2$ $[A_a = 2]$.

$$A_{CL} = \frac{V_o}{V_i} = 2.$$

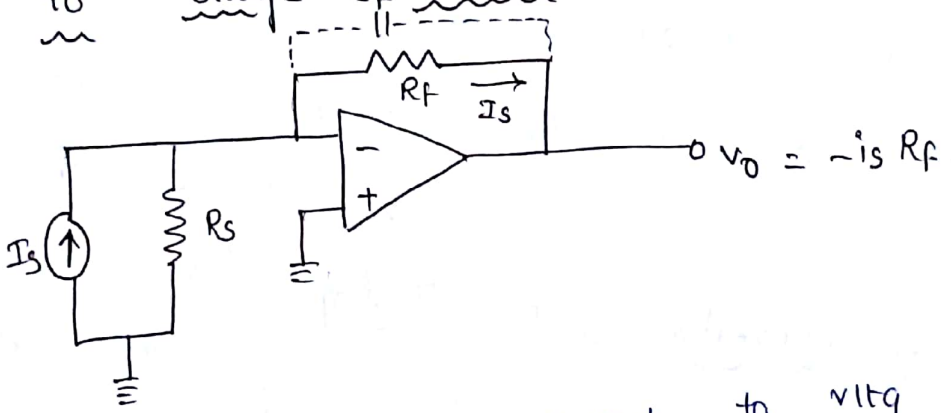
$$V_o = 2V_i$$ Sub V_1 from previous

$$V_o = V_i + V_o - I_L R$$

$$V_i = I_L R.$$

$$\boxed{V_i/R = I_L}$$

Current to voltage Converter:



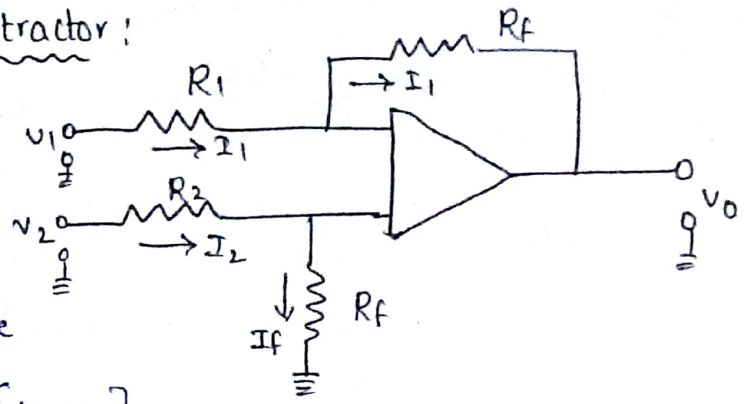
* The main purpose of current to vltg converter These convert current to voltage in photo cell, photo diode, and photo voltaic cell.

* It may be lowest current i.e., for IC741 $I_b = 3nA$.

* Sometime Cf may placed across Rf and Rc to reduce high freq noise & possibility of oscillator

These give O/P current proportional to incident radiant energy are like.

Difference Amplifier / Subtractor :

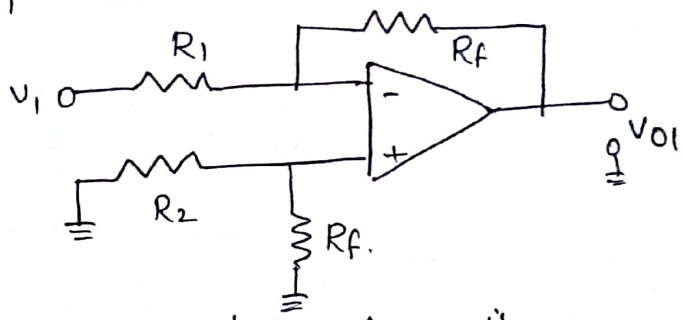


To find Relationship btw i/p's & o/p's let us use Superposition principle

* V_{o1} = o/p with V_1 $[V_2 = 0]$

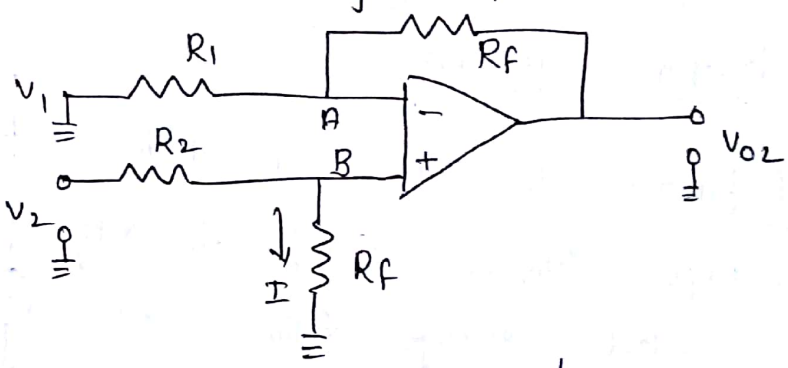
  V_{o2} = o/p with V_2 $[V_1 = 0]$

Case (i) : $V_2 = 0$ Then CKT acts as Inverting Amp & is



$$V_{o1} = -\frac{R_f}{R_1} \cdot V_1$$

Case (ii) : $V_1 = 0$ Then CKT Non-inverting Amp is



Let potential Node (B) Then potential of (A) is Same as (B).

$\therefore V_A = V_B$

Apply voltage Divider rule i/p V_2 loop

$$V_B = \frac{R_f}{R_f + R_2} \cdot V_2$$

$$I = \frac{V_B}{R_1} = \frac{V_A}{R_1} \quad \text{——— (1)}$$

$$I = \frac{V_{o2} - V_A}{R_f} = \frac{V_{o2} - V_B}{R_f} \quad \text{——— (2)}$$

(1) = (2)

$$\frac{V_B}{R_1} = \frac{V_{o2} - V_B}{R_f}$$

$$\frac{V_B R_f}{R_1} + V_B = V_{o2}$$

$$\left[1+\frac{R_f}{R_1}\right]\frac{V_2 R_f}{R_f+R_2} = V_{02}$$

Using Superposition principle $V_{01} + V_{02} = V_0$

$$V_0 = \frac{-R_f}{R_1} V_1 + \left(1+\frac{R_f}{R_1}\right)\left(\frac{R_f}{R_f+R_2}\right) V_2$$

If $R_1 = R_2$

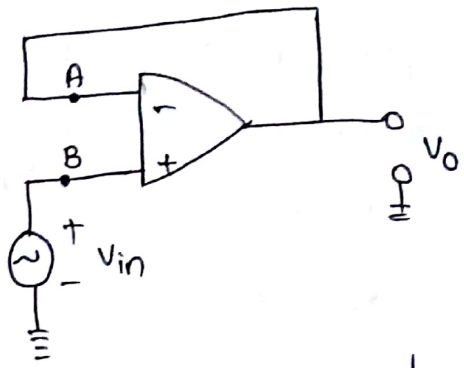
$$V_0 = \frac{-R_f}{R_1} V_1 + \left(1+\frac{R_f}{R_1}\right)\left(\frac{R_f}{R_f+R_1}\right) V_2$$

$$= \frac{-R_f}{R_1} V_1 + \frac{R_f}{R_1} V_2 = \frac{R_f}{R_1}(V_2 - V_1)$$

$R_1 = R_2 = R_f$

$$\boxed{V_0 = \frac{R_f}{R_f}(V_2 - V_1) = V_2 - V_1.}$$

Buffer Voltage:



Definition: The CKT in which o/p voltage follower CKT / i/p vltg is called voltage follower CKT Buffer CKT.

* At node (B) potential V_{in}, now At node (A) also at same potential as B, i.e., V_{in}

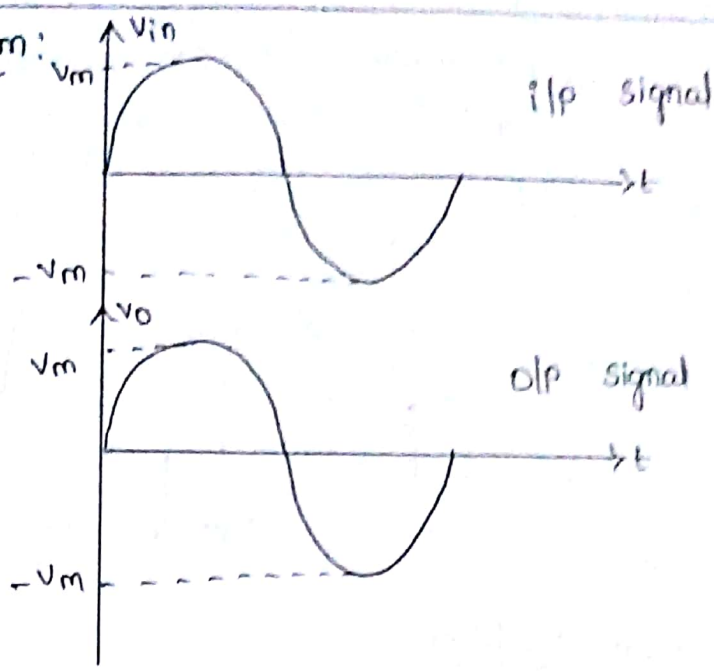
$$V_A = V_B = V_{in}$$

* Node (A) directly Connected to o/p then o/p V_0 is

$$V_0 = V_A = V_{in}.$$

* For this CKT voltage Gain is Unity.
* This is called as Unity Gain Amp, Buffer Amp, Isolation Amp, Source follower Amp.

I/p and o/p Wave form:



Advantages:

1. Very large i/p Resistance.
2. Low o/p impedance. Hence it connected to high impedance source to low impedance load as buffer.
3. Large BW. O/p follows i/p exactly without phase shift

Practical Voltage follower:

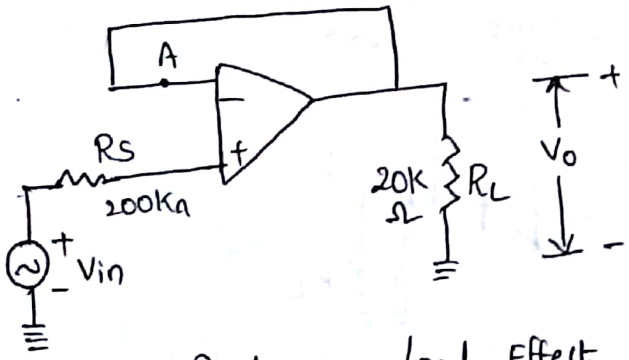
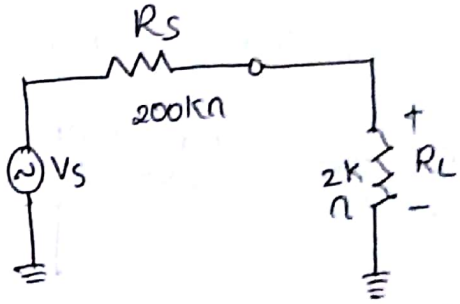


Fig a) Reducing Load Effect



b) Source driving Load

$$V_o = \frac{V_s R_L}{R_s + R_L}$$

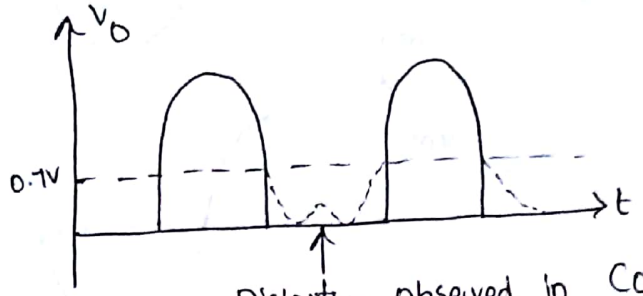
$$= \simeq 0.01 V_s$$

$V_o = V_s$.

Non - Linear function Generator:

Precision Rectifier: The o/p of conventional rectifier is distorted to reduce that distortion by using OP-Amp Ntwk called So.

These are used precisely rectify voltage having Amp. less than 0.7 V, Hence these ckt's are called Small signal precision Rectifier.

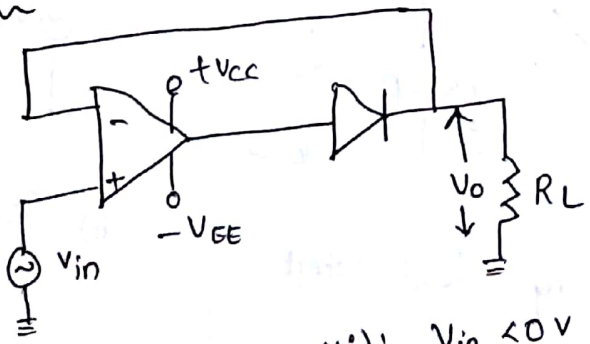


Distortion observed in Conventional Rectifier.

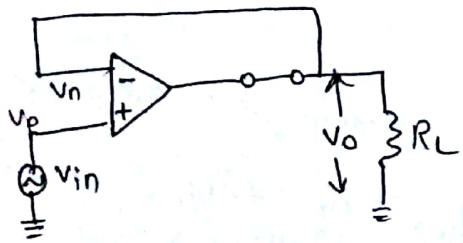
Precision Rectifier:

- Precision Rectifier
  - precision half wave
    - +ve precision half wave Rect
    - -ve precision half wave Rect
  - precision full wave
    - +ve precision full wave Rect
    - -ve precision full wave Rect

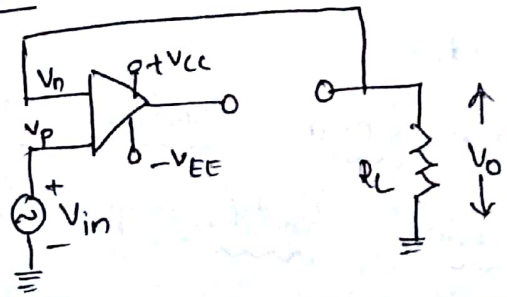
Positive precision : Half - Wave Rectifier :

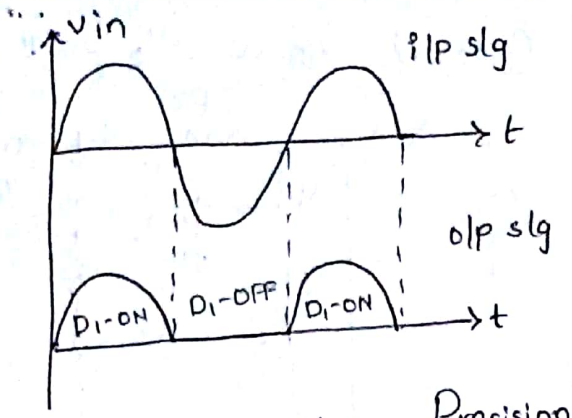


Case(i): $V_{in} > 0V$; $V_o = V_{in}$



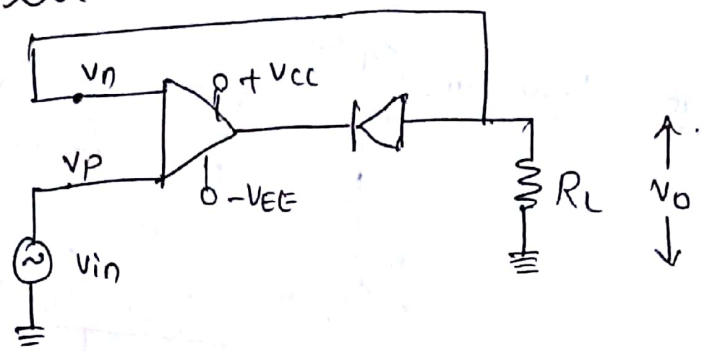
Case(ii): $V_{in} < 0V$ $V_o = 0V$.



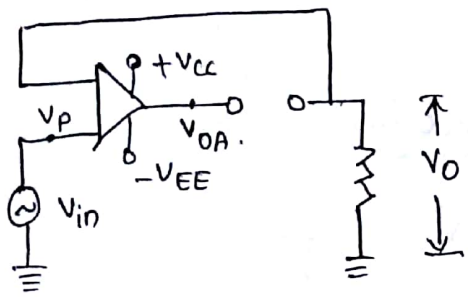


For +ve i/p cycle the +ve half cycle exist at o/p hence CKT is also known as Non - Inverting Half Wave P.R.

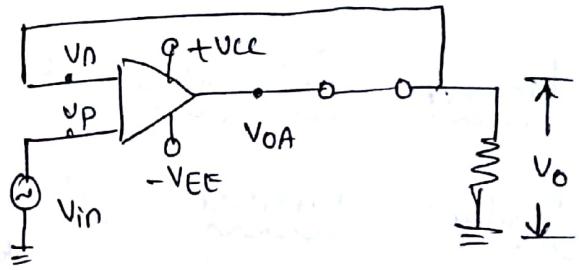
Negative Half Wave Precision:



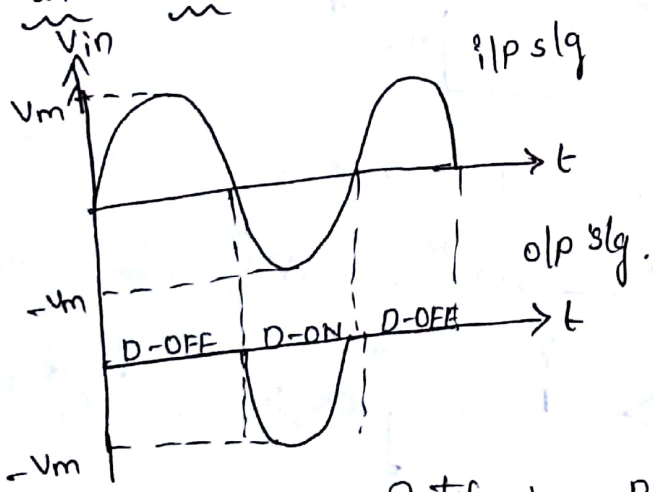
Case (i): $V_{in} > 0$; $V_o = 0$.



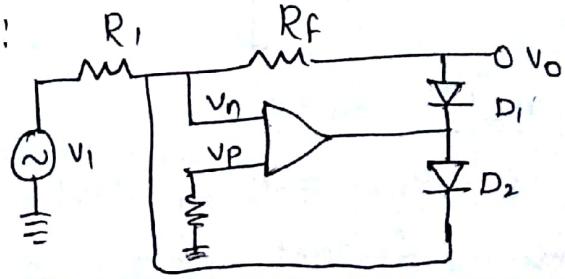
case (ii): $V_{in} < 0$; $V_o = V_{in}$



I/p and o/p Waveforms:

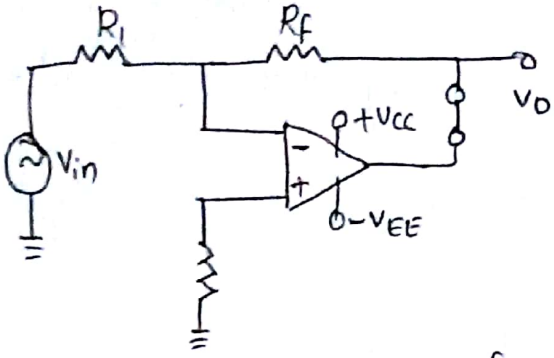


Inverting Half Wave Rectifier:

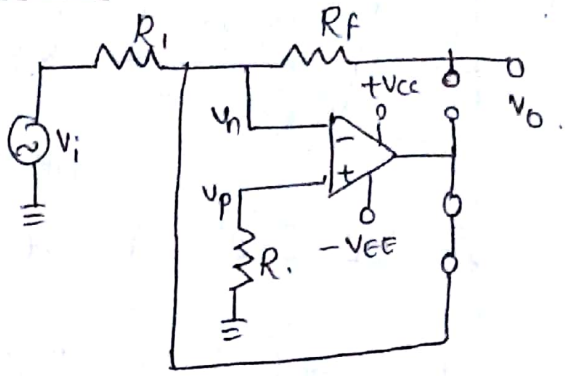


Case(i): $V_{in} > 0$ $\quad V_o = \frac{R_f}{R_1} = V_{in}$

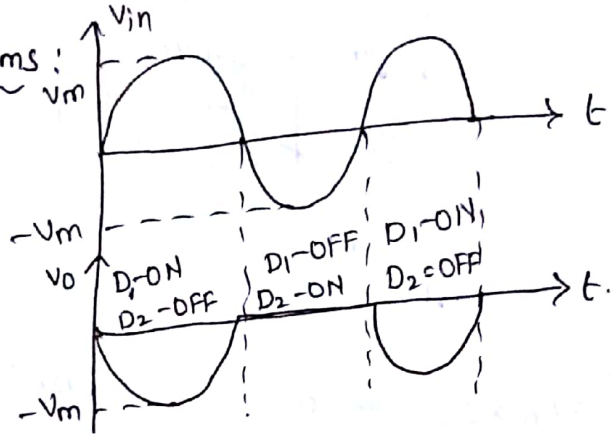
$V_o = -V_{in}$



Case(ii): $V_{in} < 0$ $\quad V_o = 0V$

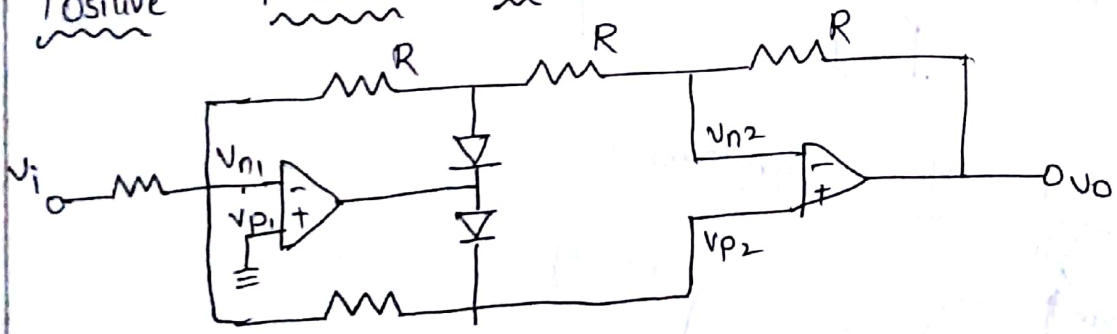


Input - Output Waveforms:



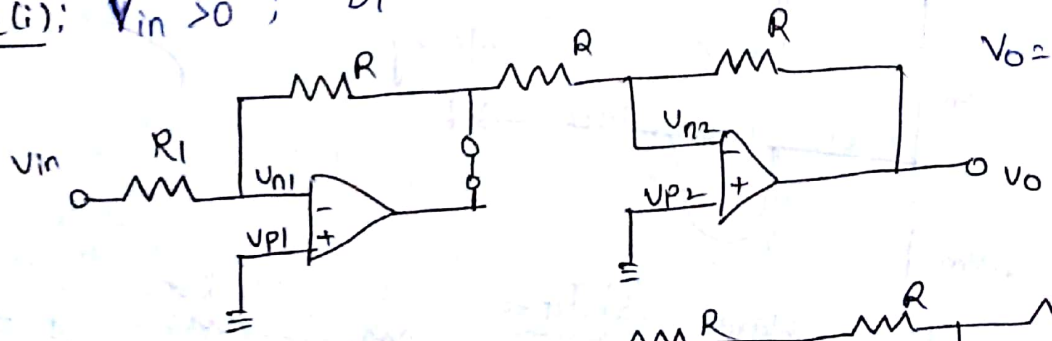
Precision full Wave Rectifier:

Positive Precision full Wave Rectifier:



Case(i): $V_{in} > 0$; $D_1 \rightarrow F/B$; short ckt ; D_2 - open - R/B

$V_o = V_i$

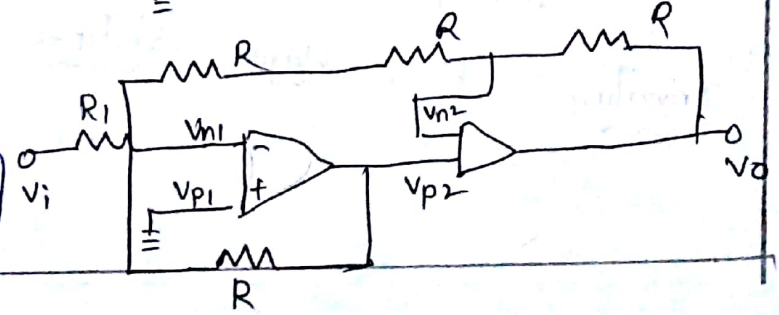


Case(ii): $V_{in} < 0$

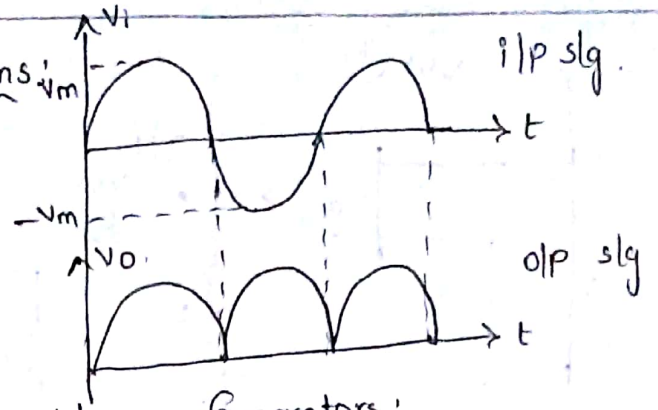
D_1 - R/B - open

D_2 - F/B - short

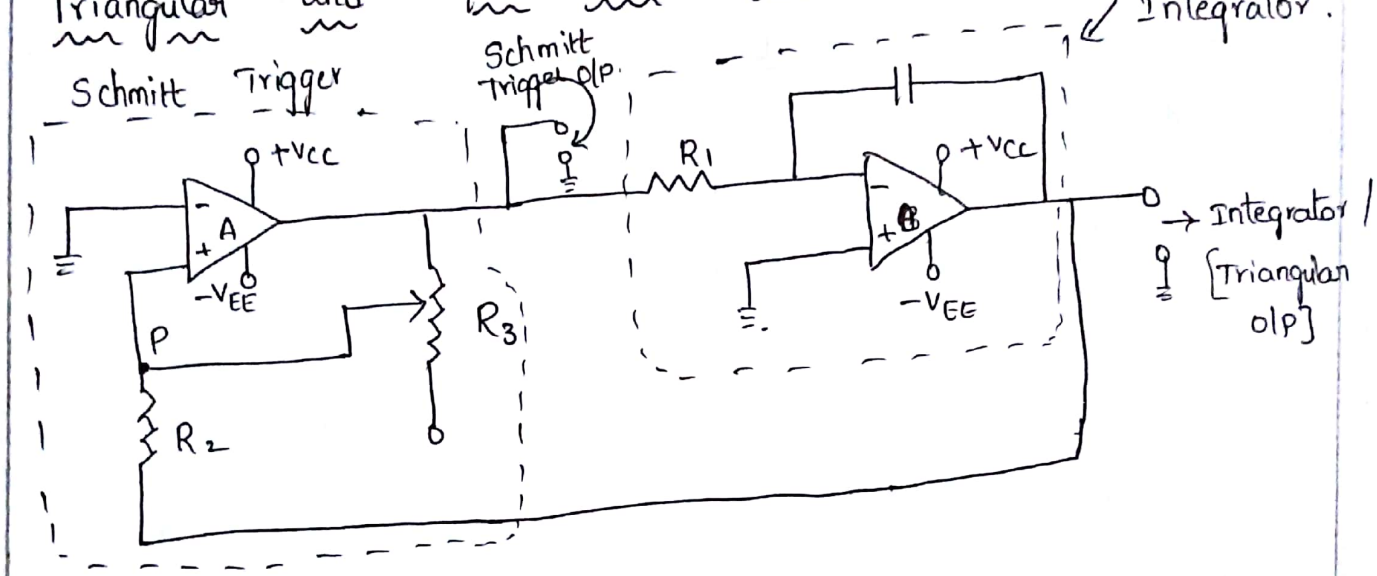
$\boxed{V_o = -V_i}$

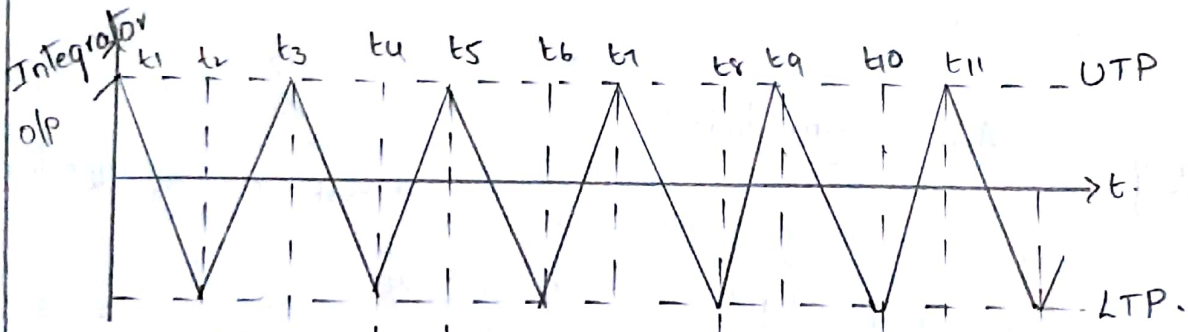


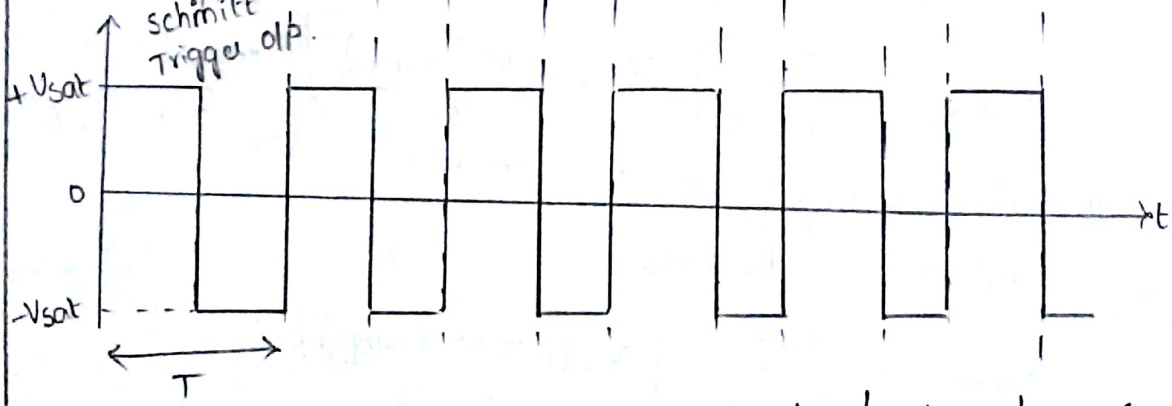
Input - Output Waveforms:



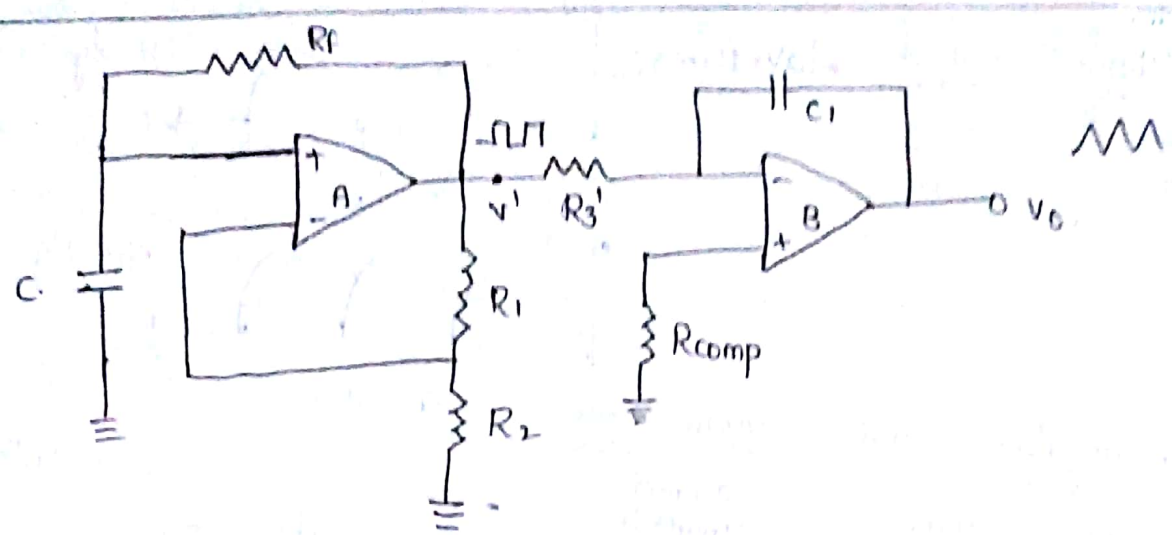
Triangular and Square Wave Generators:

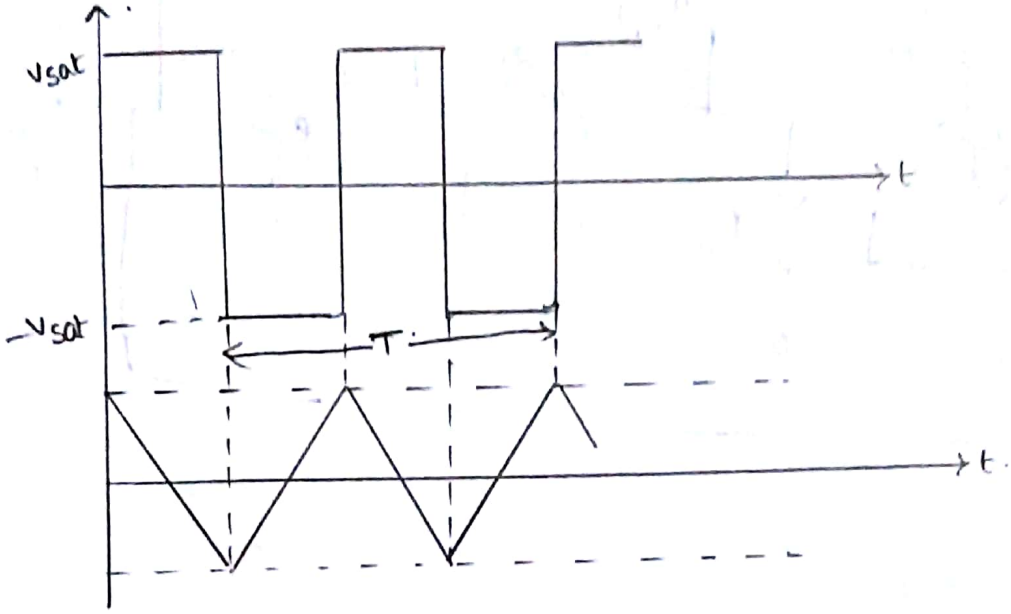






Another form of function Generator / Triangular - square Gen:





frequency And Amplitude :

* When schmitt Trigger o/p is at $+V_{sat}$, the Effective Voltage at point "p". is given by

$$-V_{Ramp} + \frac{R_2}{R_2+R_3}\left[V_{sat} - (-V_{ramp})\right] \quad \text{—} (1).$$

* When Effective Voltage at "p" becomes equal to zero. the eq^n (1) becomes.

$$-V_{Ramp} + \frac{R_2}{R_2+R_3}\left[V_{sat} - (-V_{ramp})\right] = 0.$$

Calculate V_{Ramp} :

$$-V_{ramp} + \frac{R_2}{R_2+R_3} V_{sat} + \frac{R_2}{R_2+R_3} V_{ramp} = 0$$

$$V_{ramp}\left[\frac{R_2}{R_2+R_3} - 1\right] = \frac{-R_2}{R_2+R_3} V_{sat}$$

$$-V_{ramp}\left[\frac{R_3}{R_2+R_3}\right] = \frac{-R_2}{R_2+R_3} V_{sat}$$

$$-V_{ramp} = \frac{-R_2}{R_3} V_{sat}.$$

Similarly, When schmitt Trigger o/p is at $-V_{sat}$

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}).$$

The peak to peak Amp of Triangular wave given by

$$V_o(P-P) = +V_{ramp} - (-V_{ramp})$$

$$= \frac{-R_2}{R_3}(-V_{sat}) - \left(\frac{-R_2}{R_3} V_{sat}\right)$$

$\because$ K.T $\quad |V_{sat}| = |-V_{sat}|.$

$$V_o(P-P) = \frac{R_2}{R_3}[V_{sat}] + \frac{R_2}{R_3} V_{sat} = \frac{2R_2}{R_3} V_{sat}.$$

Then $V_o(P-P)$ given by $\frac{-1}{R_1 C_1}\int_0^{T/2} -V_{sat}\, dt$

$$V_o(P-P) = \frac{-1}{R_1 C_1}[-V_{sat}]\left(T/2\right)$$

$$= \frac{V_{sat}.(T)}{2R_1C_1}$$

$$\boxed{T = \frac{2\, V_o(P-P)\, R_1 C_1}{V_{sat}.}}$$

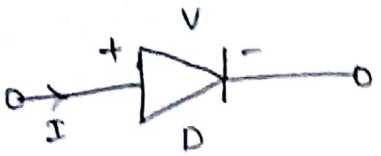
Sub, $V_o(P-P)$

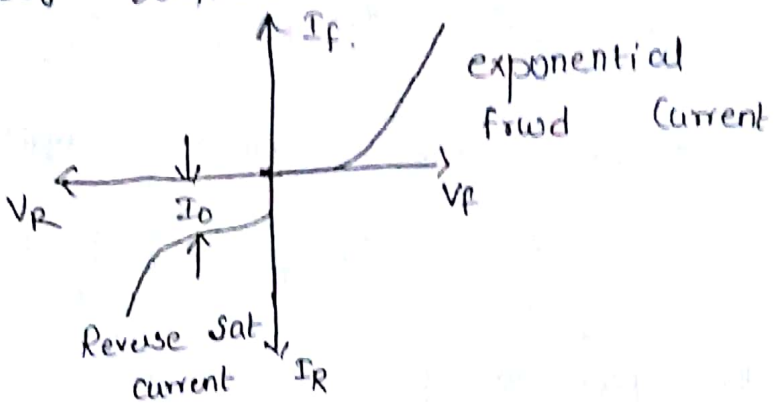
$$T = \frac{2\left(2R_2/R_3\ V_{sat}\right) R_1 C_1}{V_{sat}} = \frac{4R_2}{R_3} R_1 C_1$$

$$T = \frac{1}{f}$$

$$\boxed{f_0 = \frac{R_3}{4 R_2 R_1 C_1}} \rightarrow \text{frequency of Oscillations.}$$

Fundamentals of Log Amplifiers:





$$I_0 = I\left(e^{V/\eta V_T} - 1\right).$$

$I_f = I$ = Diode Current

V = Diode vltg

V_T = vltg eq. Temp. $\quad K = 8.62 \times 10^{-5}$ ev/°K.

$\eta = 2$ for Si

$= 1$ for Ge

If $1 <<< e^{V/\eta V_T}$

$$I_f = I_0 \cdot e^{V/\eta V_T}$$

We know that forward Current, Increases exponentially with respect to bias (V) then

$$I_f = I_0 e^{V/\eta V_T}$$

Take log on both sides.

$$\ln(I_f) = \ln\left(I_0 e^{V/\eta V_T}\right)$$

$$= \ln(I_0) + \ln e^{V/\eta V_T}$$

$$\ln\left[\frac{I_f}{I_0}\right] = \frac{V}{\eta V_T}$$

$$V = \eta V_T \ln\left[\frac{I_f}{I_0}\right]$$

This Eq^n for Diode.

The Eq^n for Transistor given

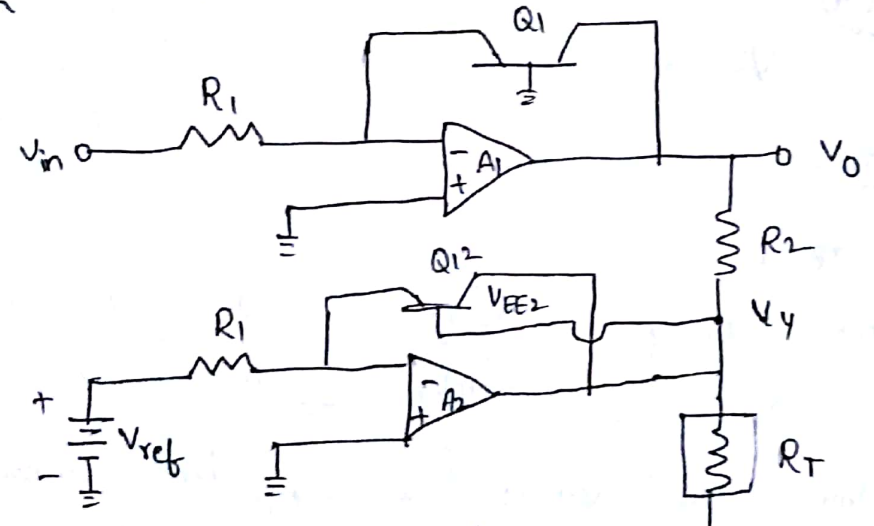
$$I_C = \alpha I_S \left(e^{V_{BE}/V_T} - 1\right)$$

$$\frac{I_C}{I_S} = \left(e^{V_{BE}/V_T} - 1\right)$$

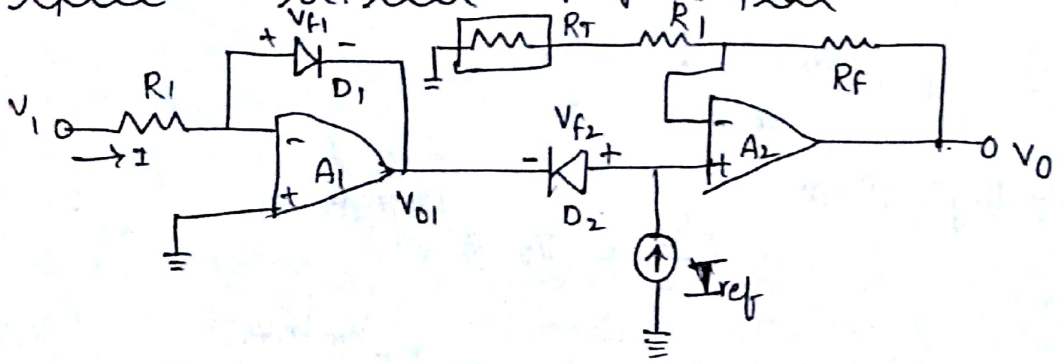
$$\ln\left[\frac{I_C}{I_S}\right] = \ln e^{V_B/V_T}$$

$$V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right) \quad \text{— ① Basic Eq}^n \text{ Tran}$$

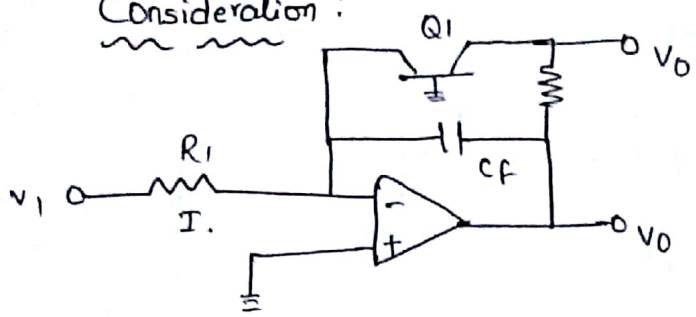
Modified Temperature Compensation Network :



Temperature Compensated Log Amplifier :



Stability Consideration :

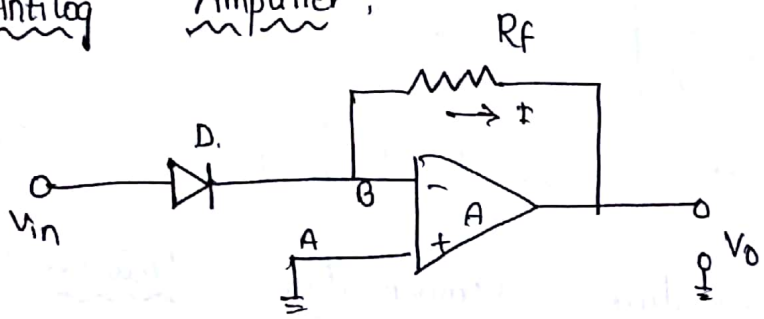


Antilog Amplifiers :

Antilog Amplifiers are classified into two Types

1) Using Diode 2) Using Transistor.

Basic Antilog Amplifier ;



At Node (A) :

$$V_A = 0.$$

At Node (B) :

$$V_B = 0.$$

The Current flowing through Diode is I_f then

$$I_f = I_0 \, e^{V_{in}/\eta V_T} \quad \text{—— (1)}$$

As op-Amp i/p current is 0, but Current "I" must be Equal to I_f.

$$I = I_f = \frac{V_B - V_0}{R_f} = \frac{-V_0}{R_f} \quad \text{—— (2).}$$

Equating (1) = (2)

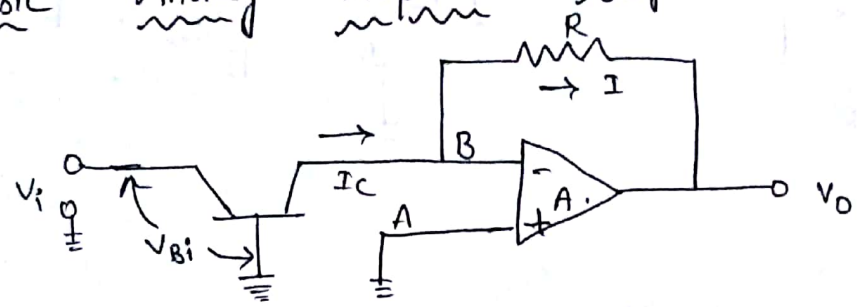
$$\frac{-V_0}{R_f} = I_0 \, e^{V_{in}/\eta V_T}$$

$$V_0 = (-I_0 R_f) \, e^{V_{in}/\eta V_T}.$$

$$V_o = -V_{ref} \cdot e^{V_{in}/\eta V_T}$$

$$V_{ref} = I_o R_f.$$

Basic Antilog Amplifier Using Transistor:



At Node A : $V_A = 0$

At Node B : $V_B = 0$

The Current through Transistor is I_C

$$I_C = I_S \cdot e^{V_{BE}/V_T}$$

$$V_{BE} = V_{in}$$

$$I_C = I_S \, e^{V_{in}/V_T} \quad \text{——— (1)}$$

$$I = I_C = \frac{V_B - V_o}{R_f} = \frac{-V_o}{R_f} \quad \text{——— (2)}$$

Equate (1) & (2)

$$\frac{-V_o}{R_f} = I_S \, e^{V_{in}/V_T}$$

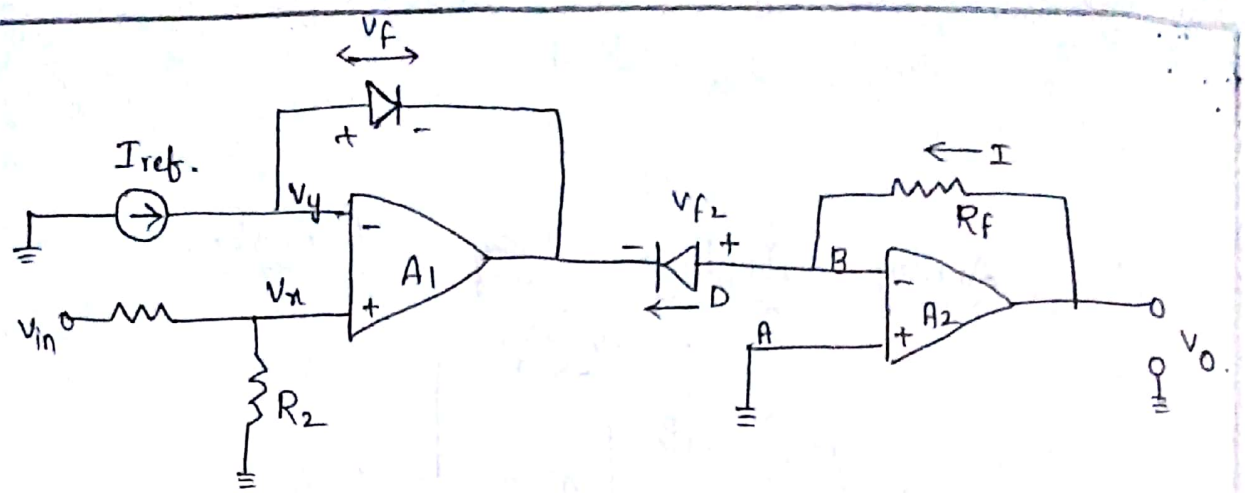
$$V_o = -I_S R_f \, e^{V_{in}/V_T}$$

$$= -V_{ref} \cdot e^{V_{in}/V_T}$$

$$\boxed{V_{ref} = I_S \cdot R_f}$$

Temperature Compensated Antilog Amplifier:

Let Vltg at non-inverting terminal of V_x of OPAmp A_1, V_1, V_x.



$$V_x = \frac{R_2}{R_2+R_1} V_{in}$$

$$V_x = \frac{R_2}{R_2+R_1} V_{in}.$$

The o/p vltg is given by $V_{01} = V_x - V_{f1}$

W.K.T $V_{f1} = \eta V_T \ln\left[\frac{I_f}{I_0}\right]$

$$V_{01} = \frac{R_2}{R_1+R_2} V_{in} - \eta V_T \ln\left[\frac{I_f}{I_0}\right] \quad \text{—— (1)}$$

$$V_{01} = -V_{f2}.$$

$$V_{01} = -V_{f2}$$

$$V_{f2} = \eta V_T \ln\left[\frac{I_{f2}}{I_0}\right] \quad \text{—— (2)}$$

$$I_{f2} = I = \frac{V_0 - V_B}{R_f} = \frac{V_0}{R_f}.$$

$$I_{f1} = I_{ref}.$$

then $V_{01} = -\eta V_T \ln\left[\frac{V_0}{I_0 R_f}\right]$ —— (3).

$$V_{in}\left[\frac{R_2}{R_1+R_2}\right] - \eta V_T \ln\left[\frac{I_{ref}}{I_0}\right] = -\eta V_T \ln\left[\frac{V_0}{R_f I_0}\right]$$

$$V_{in}\left[\frac{R_2}{R_1+R_2}\right] = \eta V_T \left[\ln(I_{ref}) - \ln I_0\right] - \ln\left[V_0/R_f\right] + \ln(I_0)$$

$$\therefore V_{in}\left(\frac{R_2}{R_1+R_2}\right) = \eta V_T \ln\left[\frac{I_{ref}\cdot R_f}{V_o}\right] = -\eta V_T \ln\left[\frac{V_o}{I_{ref}\cdot R_f}\right]$$

$$V_o = I_{ref}\cdot R_f \ln^{-1}\left[\frac{V_{in} R_2}{\eta V_T (R_1+R_2)}\right]$$

Multivibrator Using Op-Amp :

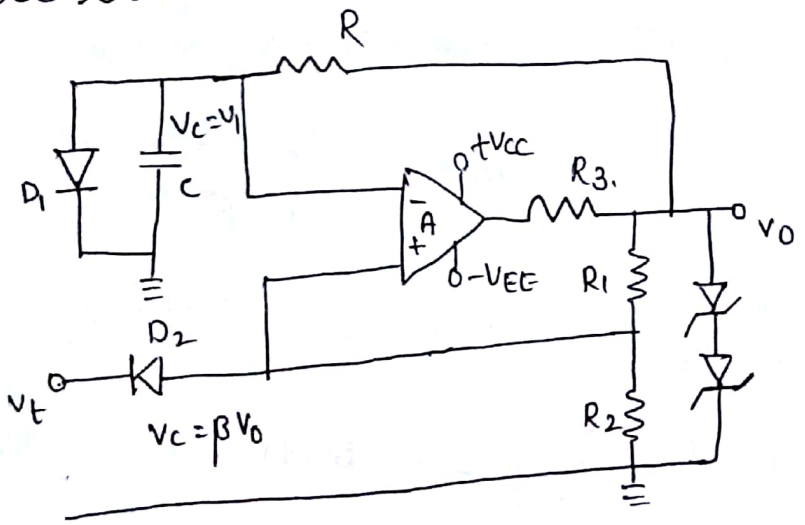
* Multivibrators are important group of Regenerative CKt that are used in Timing applications.

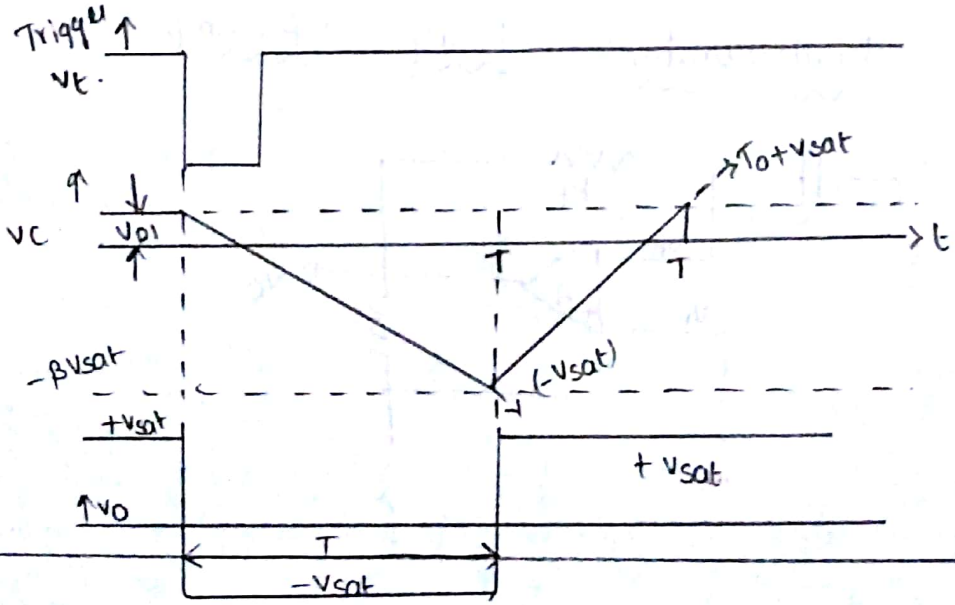
* Multivibrators non-sinusoidal waveforms generators.

  i) Mononstable Multivibrator

  ii) Astable Multivibrator

Monostable Multivibrator :





Wave for pulse Width (T) :

Low pass CKT V_i = Initial value of vltg.

V_f = Final value of vltg.

$$V_o = V_f + (V_i - V_f)\, e^{-t/RC} \quad \text{—— (1)}$$

For Monostable, $V_f = -V_{sat}$ $V_i = V_{d1}$

$$V_C = -V_{sat} + (V_{d1} + V_{sat})\, e^{-t/RC}$$

But at $t = T$ $V_C = -\beta V_{sat}$.

$$-\beta V_{sat} = -V_{sat} + (V_{d1} + V_{sat})\, e^{-T/RC}$$

$$V_{sat}(1-\beta) = (V_{d1} + V_{sat})\, e^{-T/RC}$$

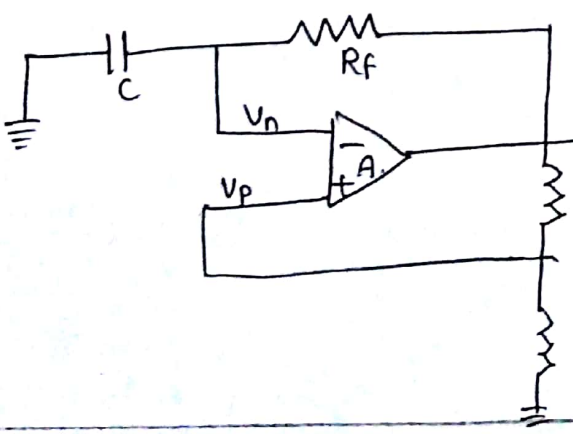
$$e^{-T/RC} = V_{sat}(1-\beta) / V_{d1} + V_{sat}.$$

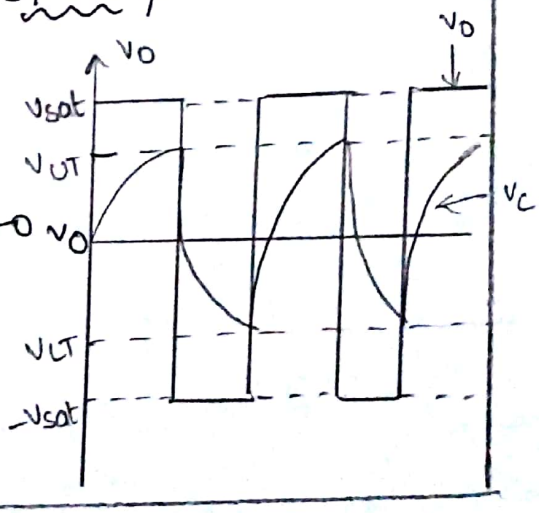
$$T = RC \ln\left[\frac{V_{D1}/V_{sat} + 1}{1-\beta}\right].$$

$\beta = \frac{R_2}{R_2 + R_1}$ $V_{sat} >> V_{D1}$ & $R_1 = R_2$ $\beta = 0.5$

$$T = RC \ln\left[\frac{1}{1-0.5}\right] = RC \ln(2) = RC.(0.69).$$

Astable Multivibrator Using OP-Amp :





* The o/p vltg (V_0) at $+V_{sat}$. The F/B vltg called Upper Threshold voltage. (V_{UT}) & given by

$$V_{UT} = \frac{R_1(+V_{sat})}{R_1+R_2}$$

$$V_{LT} = \frac{R_1(-V_{sat})}{R_1+R_2}.$$

Derivation of frequency of Oscillation:

The freq. of Oscillation is time it takes capacitor to charge from V_{UT} to V_{LT}

$$V_c(t) = V_{max} + (V_{initial} - V_{max})\, e^{-t/T}$$

where $V_c(t) \rightarrow$ Instaneous vltg across cap.

$V_{initial} \rightarrow$ Initial vltg.

$V_{max} \rightarrow$ vltg. towards which cap is chargin

$$V_{UT} = V_{sat} + (V_{LT} - (+V_{sat}))\, e^{-T_1/R_fC}.$$

$$(V_{LT} - V_{sat})\, e^{-T_1/R_fC} = V_{UT} - V_{sat}$$

$$-T_1 = R_f C \ln\left[\frac{V_{sat} - V_{UT}}{V_{sat} - V_{LT}}\right]$$

$$T_1 = R_fC \ln\left(\frac{1 - V_{LT}/V_{sat}}{1 - V_{UT}/V_{sat}}\right)$$

at $T = 2T_1$

$$= 2\left[R_f C \ln\left(\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}\right)\right].$$

$$f_0 = 1/2R_fC \ln\left[\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}\right].$$

$$f_0 = \frac{1}{2R_fC \ln\left[\dfrac{V_{sat} - R_1(-V_{sat})/R_1+R_2}{V_{sat} - R_1(V_{sat})/R_1+R_2}\right]}$$

$$= \frac{1}{2R_fC} \ln\left[\frac{V_{sat}\left(1+\frac{R_1}{R_1+R_2}\right)}{V_{sat}\left(1-\frac{R_1}{R_1+R_2}\right)}\right]$$

$$f_0 = \frac{1}{2R_fC} \ln\left[\frac{2R_1+R_2}{R_2}\right]$$

COMPARATOR:

* A comparator is CKT which compare signal vltg applied at one i/p of OP-Amp with known ref. voltage at other i/p.
* It is basically open-loop op-Amp with o/p $\pm V_{sat}$.

Transfer characteristics of Ideal and practical OP-Amp:

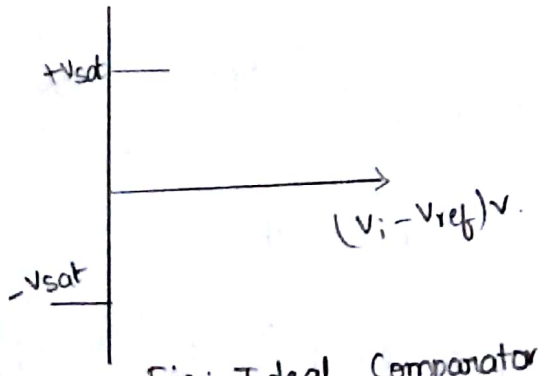


Fig: Ideal Comparator

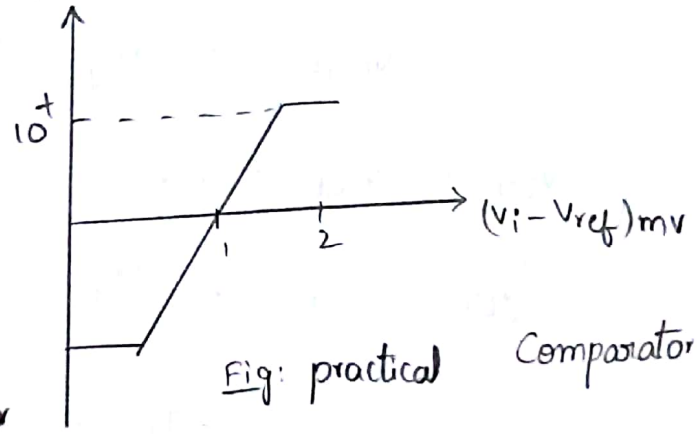


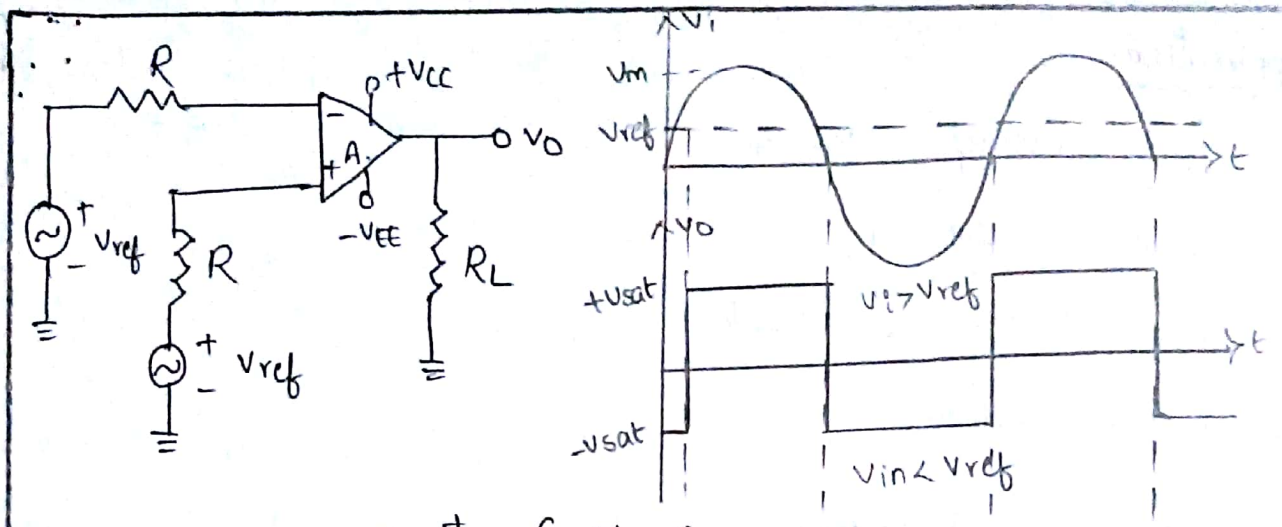
Fig: practical Comparator

Classification of Comparators:

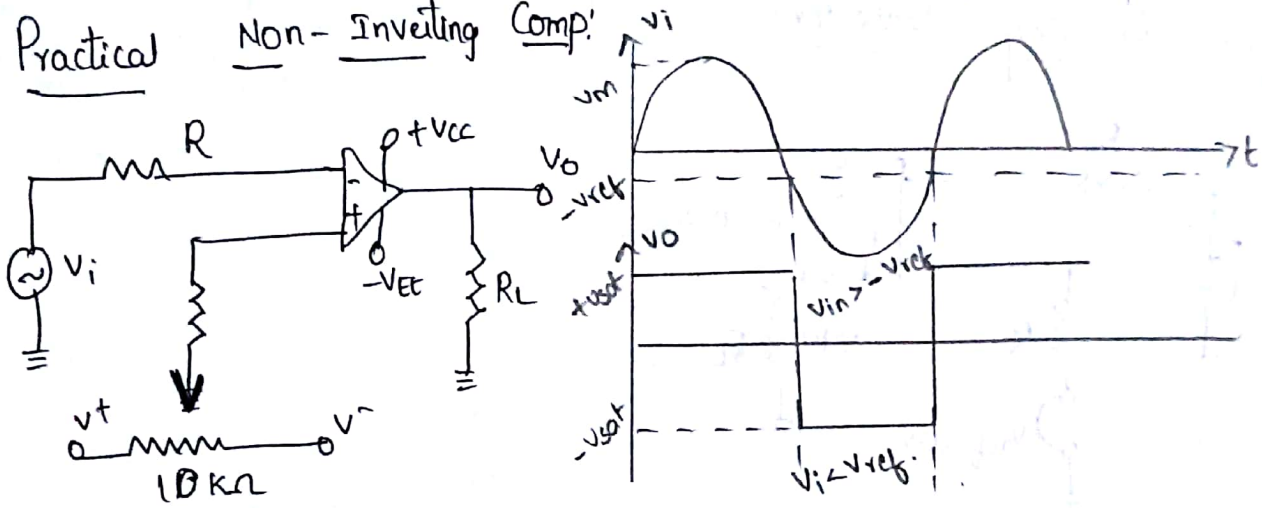
* There are basically 2 Types of comparator

1. Non-Inverting Comparator
2. Inverting Comparator.

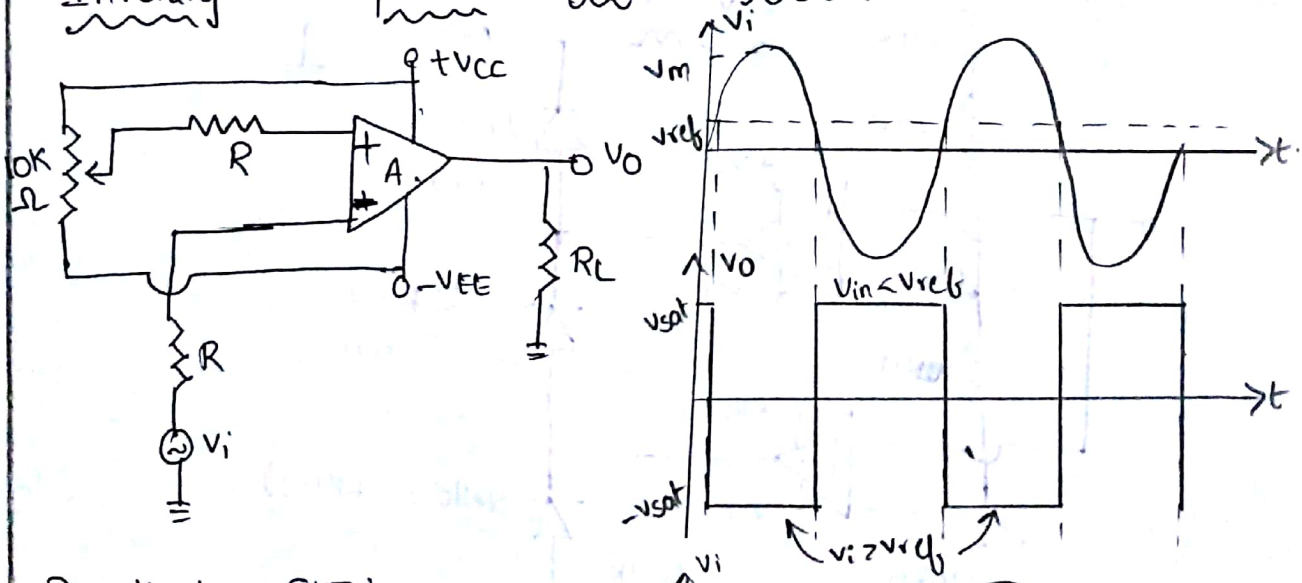
Non-Inverting Comparator / Basic Non-inverting Comparator



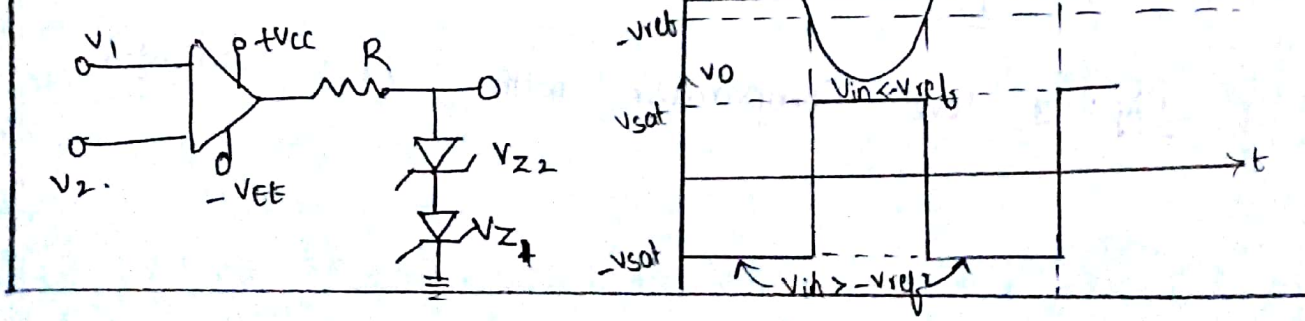
Practical Non-Inverting Comp:



Inverting Comparator / Basic Inverting Comparator:



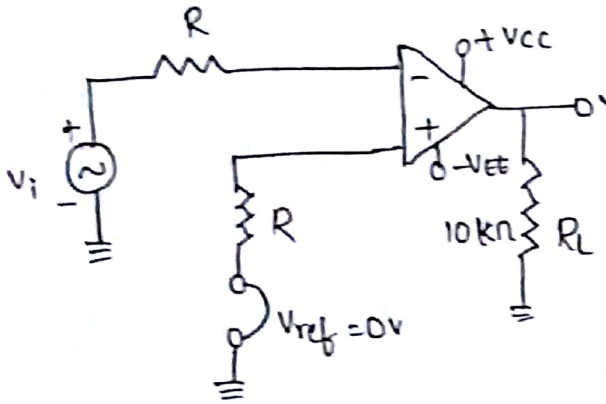
Practical CKT:

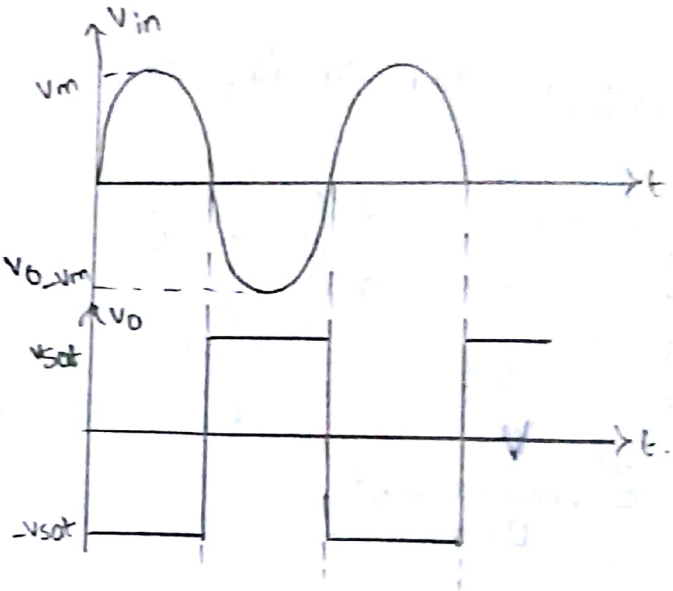


Applications:

1. Zero Crossing Detector
2. Window Detector
3. Time - Marker Generator
4. phase Detector.

Zero - Crossing Detector:





Window Detector:

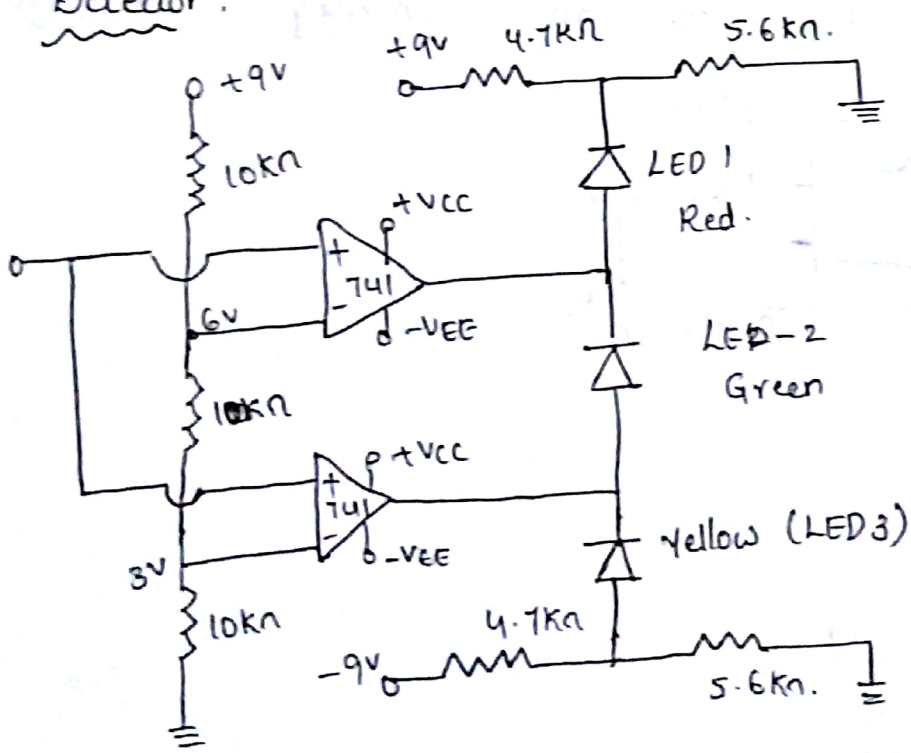
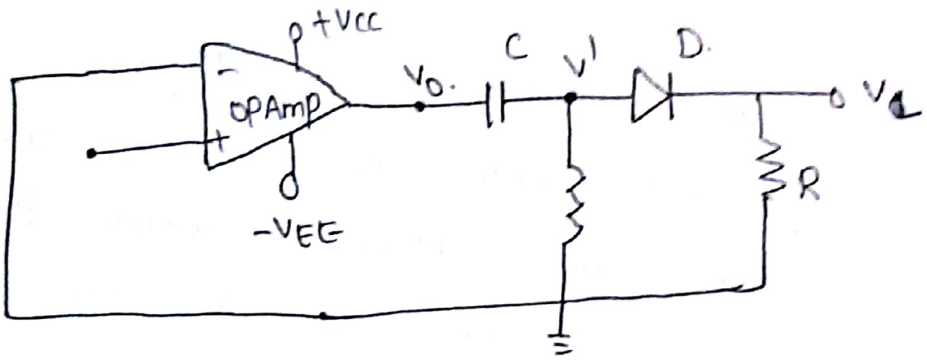


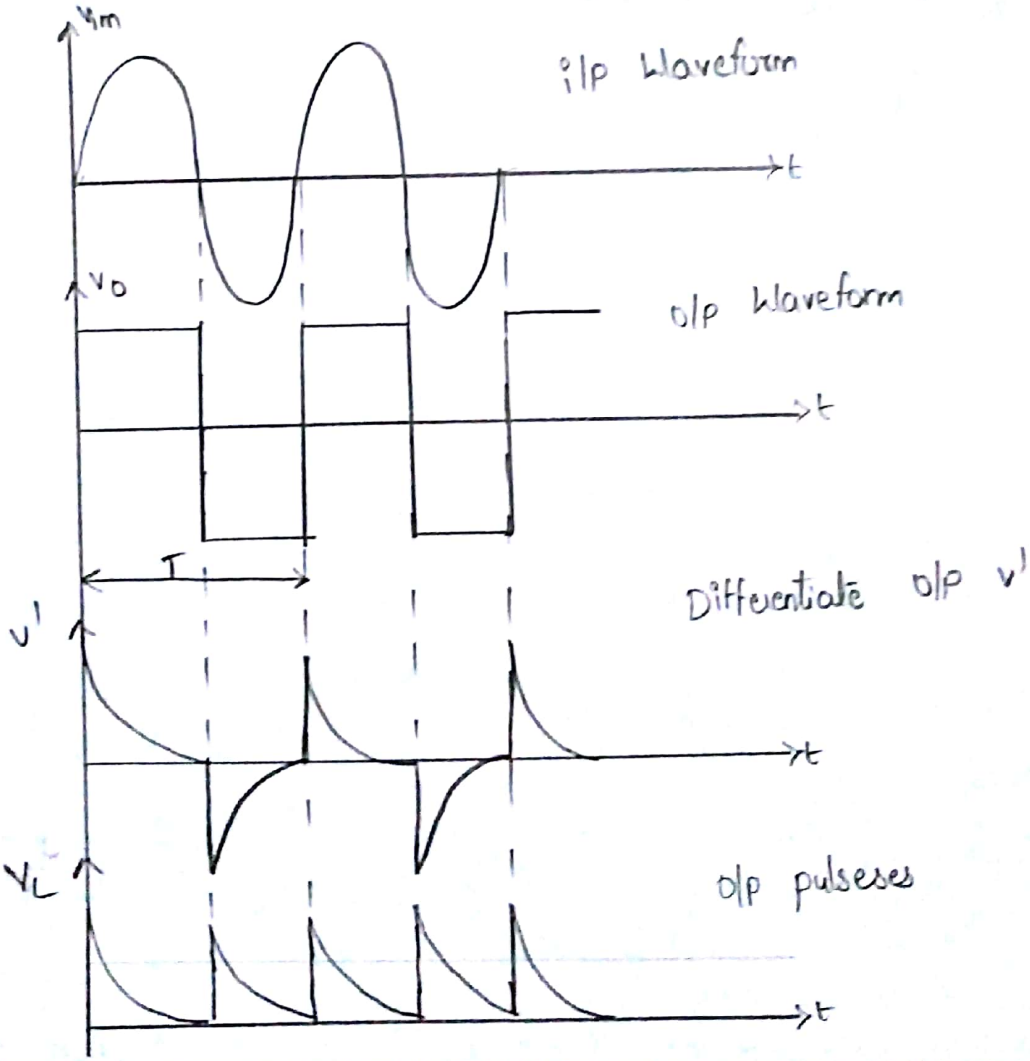
Fig: 3 - level Comparator with LED indicator.

I/p (V_{OH})	Yellow LED3	Green LED2	RED LED1
Less than 3v	ON	OFF	OFF
Btw 3 and 6v	OFF	ON	OFF
Greater than 6V	OFF	OFF	ON

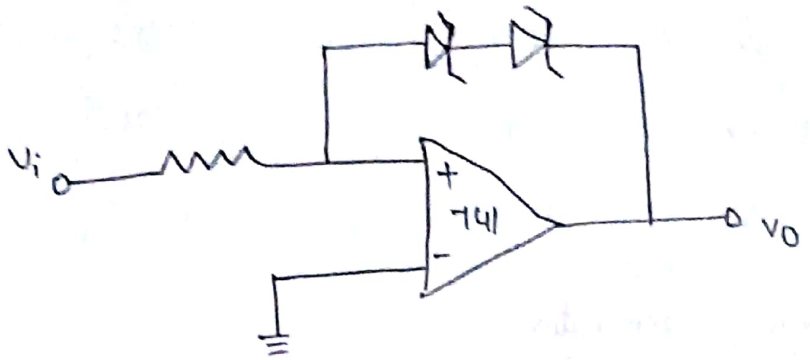
Time Marker Generator:



i/p and o/p Waves:



Phase Detector :



Definition :

* The phase Angle between two voltages can be measured using CKT. Both voltages are converted into spikes and time interval between pulse spikes of one i/p and that of other is measured.

* The time interval is proportional to phase difference :

UNIT - IV

Active Filters; ANALOG MULTIPLIERS AND MODULATORS :

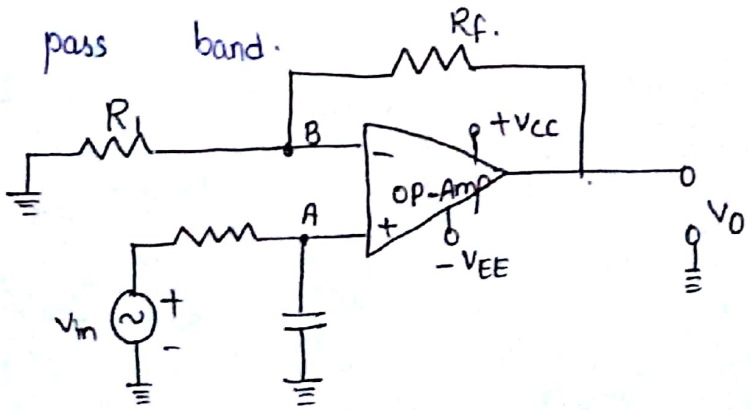
Design and Analysis of Butterworth Active Filter :

* The various types of filters used in practice which approximately produce ideal response are :

1. Butterworth filters.
2. Chebyshev filter
3. Cauer filters.

Design Steps for the First order Low pass Butterworth filter :

* The first order Lowpass Butterworth filter is realised by RC circuit used along with an op-Amp used in non-inverting Configuration.
* This is also called "One pole Low pass Butterworth filter."
* The Resistance R_f and R_1 decide the gain of filter in pass band.



Design Steps :

1. choose cut off frequency, f_H.

2. Choose capacitance C usually between 0.001 and 1μF. Generally, it is selected as 1μF or less than that. For better performance, mylar or tantalum capacitors are selected.

3. Now the RC circuit, $f_H = \frac{1}{2\pi RC}$.

   Hence as f_H and C are known, calculate value "R".

4. The R_f and R_1 can be selected depending on req. gain in pass band.

$$A_F = 1 + \frac{R_f}{R_1}$$

Analysis of filter Circuit :

The impedance of capacitor C is $-jX_C$ where X_C is the capacitive reactance given by $X_C = \frac{1}{2\pi fC}$.

By the potential divider rule, the voltage at the non-inverting input terminal A which is voltage across capacitor C is given by.

$$V_A = \frac{-jX_C}{R - jX_C} \cdot V_{in}$$

$$V_A = \frac{-j\left[1/2\pi fC\right]}{R - j\left[1/2\pi fC\right]} \cdot V_{in} = \frac{-j}{2\pi fRC - j} \cdot V_{in}$$

$$= \frac{V_{in}}{1 - \frac{2\pi fRC}{j}}$$

but $-j = 1/j$ $\quad \frac{-1}{j} = j$

$$V_A = \frac{V_{in}}{1 + j\,2\pi f RC} \quad \text{—— (2)}$$

As OP-Amp is non-inverting

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_A \quad \text{—— (3)}$$

$$V_o = \left[1 + \frac{R_f}{R_1}\right] \frac{V_{in}}{1 + j\,2\pi f RC}$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j(f/f_H)} \quad \text{—— (4)}$$

Where $A_F = \left(1 + \frac{R_f}{R_1}\right)$ = Gain of filter in pass band —— (5)

$f_H = \frac{1}{2\pi RC}$ = High cut OFF freq of filter —— (6)

f = operating freq.

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}} \quad \text{—— (7)} \; ; \; \phi = \tan^{-1}\left(\frac{f}{f_H}\right) \quad \text{—— (8)}$$

The phase angle ϕ is in degrees.

Eq (7) describes behaviour of low pass filter.

1. At very low frequencies, $f < f_H$.

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F \quad \text{i.e., constant.}$$

2. At $f = f_H$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\,A_F \quad \text{i.e., 3 dB down to level } (A_F)$$

3. At $f > f_H$.

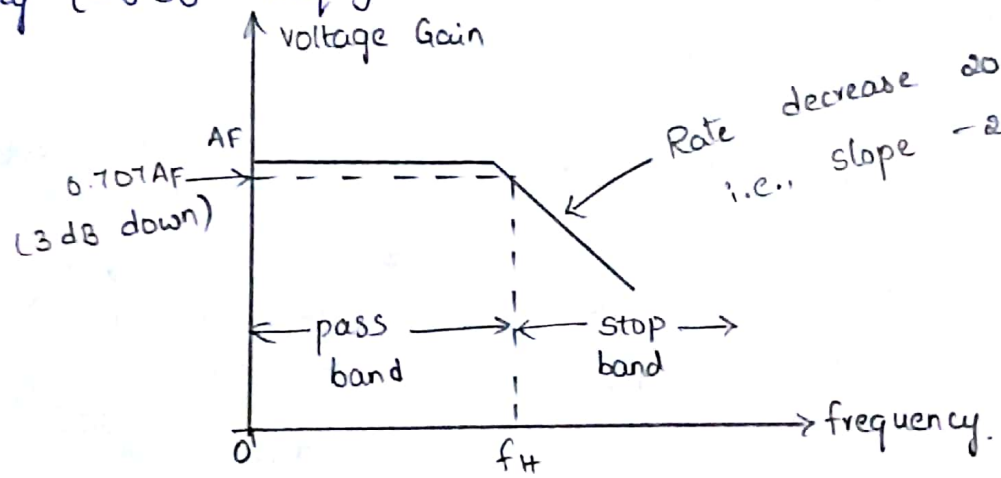
$$\left|\frac{V_o}{V_{in}}\right| < A_F.$$

* Thus for Range $0 < f < f_H$, gain almost constant equal to f_H which high cutoff frequency.

* At $f = f_H$ gain reduces to 0.707 i.e., 3 dB down from A_F. and frequency increases than f_H, gain decreases at rate of 20 dB/decade.

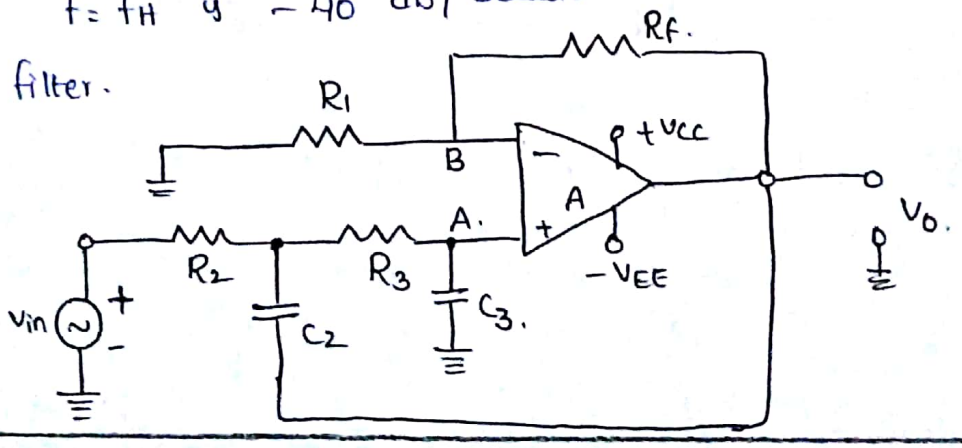
* The rate 20 dB/decade means decrease of 20 dB/gain per 10 time change in frequency. The same rate can be expressed as 6 dB/octave i.e., decrease of 6dB per two time change in frequency.

* The frequency (f_H) is called Cut-off frequency, break frequency [-3 dB freq] or Corner frequency.



Second Order Low pass Butter Worth Filter:

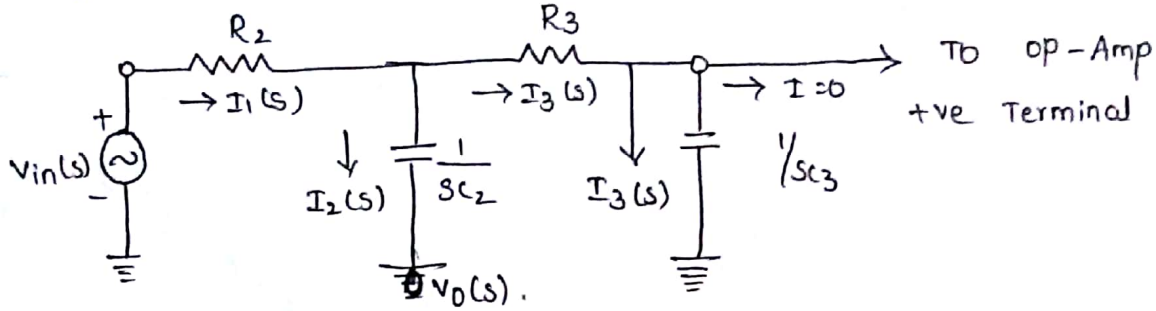
In case of Second Order filter, the gain rolls off at rate of 40 dB/decade. Thus ~~decade~~ slope of freq. response after $f = f_H$ is -40 dB/decade for second order Low pass filter.



Analysis of filter Circuit :

For deriving expression for cut-off freq, let us see laplace Transform method.

The i/p RC network can be represented in L.T.



Now $I_1 = I_2 + I_3$ —— ①.

$$\frac{V_{in} - V_1}{R_2} = \frac{V_1 - V_0}{(1/sC_2)} + \frac{V_1 - V_A}{R_3} \quad \text{—— ②}$$

using potential divider Rule, we can write

$$V_A = V_1 \left[\frac{1/sC_3}{R_3 + 1/sC_3} \right] \quad \text{—— ③.}$$

$$V_A = \frac{V_1}{1 + sR_3C_3} \quad \text{—— ④.}$$

$$V_1 = V_A(1 + sR_3C_3)$$

Sub Eq② for solving V_A, we get.

$$\frac{V_{in} - V_A(1+sR_3C_3)}{R_2} = \frac{V_A(1+sR_3C_3) - V_0}{(1/sC_2)} + \frac{V_A(1+sR_3C_3) - V_A}{R_3}.$$

$$\frac{V_{in}}{R_2} + V_0(sC_2) = V_A \left[\frac{(1+sR_3C_3)}{R_2} + sC_2(1+sR_3C_3) + \frac{1+sR_3C_3}{R_3} - \frac{1}{R_3} \right]$$

$$\frac{V_{in}}{R_2} + V_0(sC_2) = V_A \left[\frac{R_3(1+sR_3C_3) + R_2R_3\, sC_2(1+sR_3C_3) + R_2(1+sR_3C_3) - R_2}{R_2R_3} \right]$$

$$\therefore (R_3 V_{in} + V_o s R_2 R_3 C_2) = V_A \left[(1 + sR_3C_3)(R_3 + R_2R_3 sC_2 + R_2) - R_2 \right]$$

$$V_A = \frac{R_3 V_{in} + V_o s R_2 C_2 R_3}{(1+sR_3C_3)(R_3 + R_2R_3C_2 s + R_2) - R_2} \quad \text{—— (5)}$$

$$V_o = A_F V_A \quad \text{—— (6)} \qquad \left(\because A_F = 1 + \frac{R_F}{R_1} \right).$$

and V_A = The vltg at Non-inverting Terminal

$$V_o = A_F \left[\frac{R_3 V_{in} + V_o s R_2 R_3 C_2}{(1+sR_3C_3)(R_3 + R_2R_3C_2 s + R_2) - R_2} \right].$$

$$\frac{A_F R_3 V_{in}}{(1+sR_3C_3)(R_3 + R_2R_3C_2 s + R_2) - R_2} = V_o \left[1 - \frac{s R_2 R_3 C_2}{(1+sR_3C_3)(R_3 + R_3R_2 sC_2 + R_2) - R_2} \right]$$

$$A_F R_3 V_{in} = V_o \left[(1 + sR_3C_3)(R_3 + R_3R_2 sC_2 + R_2) - R_2 - sR_2R_3C_2 \right].$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{s^2 + \frac{s(R_3C_3 + R_2C_3 + R_2C_2 - A_F R_2C_2)}{R_2R_3C_2C_3} + \frac{1}{R_2R_3C_2C_3}} \quad \text{—— (7)}$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad \text{—— (8)}$$

A = Overall Gain

ξ = Damping of system

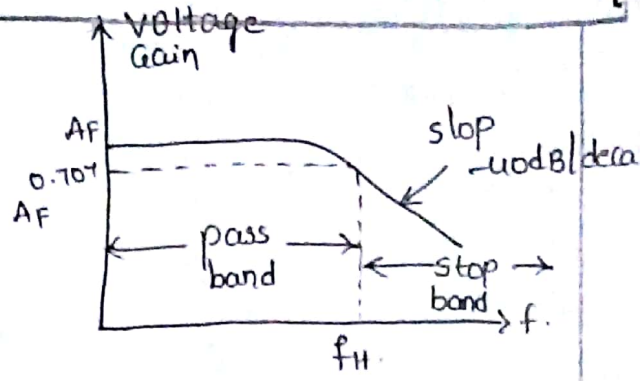
ω_n = Natural frequency of oscillation.

Compare (7) and (8).

$$\omega_n^2 = \frac{1}{R_2R_3C_2C_3} \Rightarrow \boxed{f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}} \quad \text{—— (10)}$$

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi.$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{\sqrt{1+(f/f_H)^4}}.$$



Design Steps:

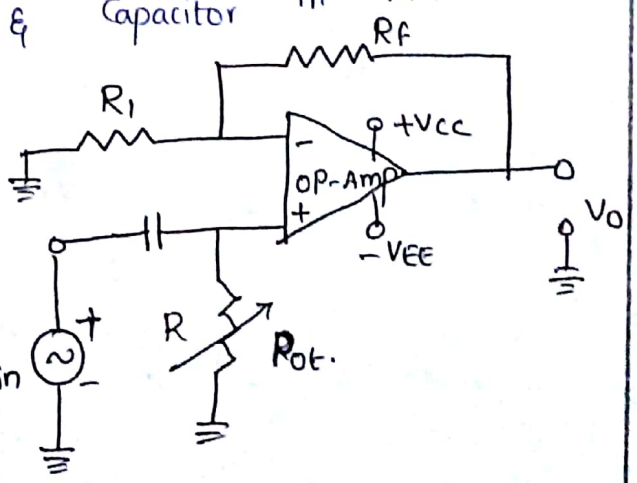
1. Choose cut off frequency f_H.
2. The design can be simplified by selecting $R_2 = R_3 = R$ and $C_2 = C_3 = C$ and choose value "C" less than (or) equal to $1\mu F$.
3. Calculate value R from Eq^n.

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi RC}$$

4. As $R_2 = R_3 = R$; $C_2 = C_3 = C$ the pass band voltage gain $A_F = (1 + R_f/R_1)$ of sec order low pass filter has to be equal to 1.586.

First Order High pass Butterworth filter:

* The high pass filter performs opposite function of low pass filter. This CKT can be obtained by interchanging the Resistor & Capacitor in LPF.



* The frequency at which gain is 0.707 times gain of filter in pass band is called Low-cut-off frequency

Analysis :

* The impedance of capacitor $-jX_C = -j\left[\frac{1}{2\pi fC}\right]$ where $f \rightarrow$ i/p i.e., operating freq.

By vltg divider Rule, potential of non-inverting Terminal of op-Amp is

$$V_A = V_{in}\left[\frac{R}{R - jX_C}\right] \quad \text{—(1)}$$

$$V_A = V_{in}\left[\frac{R}{-jX_C\left(\frac{R}{-jX_C} + 1\right)}\right] \quad \text{taking } -jX_C \text{ outside.}$$

As $\frac{-1}{j} = j$; $\frac{-1}{jX_C} = \frac{j}{X_C} = \frac{j}{1/2\pi fC} = j2\pi fC$. —(2)

$$V_A = V_{in}\left[\frac{-R/jX_C}{-R/jX_C + 1}\right]$$

$$= V_{in}\left[\frac{j2\pi fRC}{1 + j2\pi fRC}\right]$$

$$V_A = V_{in}\left[\frac{j.(f/f_L)}{1 + j(f/f_L)}\right] \text{—(3)} \quad \left(\because f_L = \frac{1}{2\pi RC}\right).$$

Now for op-Amp in non-inverting Configuration

$$V_o = V_A \cdot A_F. \quad \text{—(4)}$$

$$A_F = \left(1 + \frac{R_f}{R_1}\right) = \text{Gain of op-Amp in passband}$$

Sub (3) in (4) $\Rightarrow V_o = A_F V_{in}\left[\frac{j(f/f_L)}{1 + j(f/f_L)}\right]$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F (f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

i) Low frequencies i.e., $f < f_L \Rightarrow \left|\frac{V_o}{V_{in}}\right| < A_F$

2) $f = f_L$

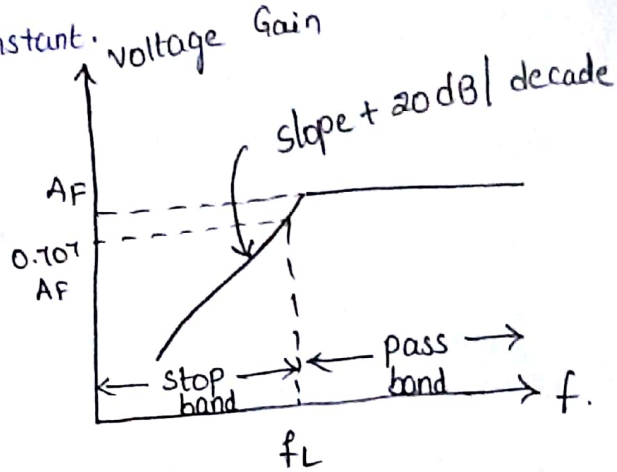
$$\left|\frac{V_o}{V_{in}}\right| = 0.707\, A_F$$ i.e., 3 dB down from level of A_F.

3) At $f > f_L$ i.e., high frequencies, 1 can be neglected compared to (f/f_L) from denominator.

$$\left|\frac{V_o}{V_{in}}\right| = A_F$$ i.e., Constant voltage Gain

For the freq, $f < f_L$ the gain increases till $f = f_L$ at rate of +20 dB/decade.

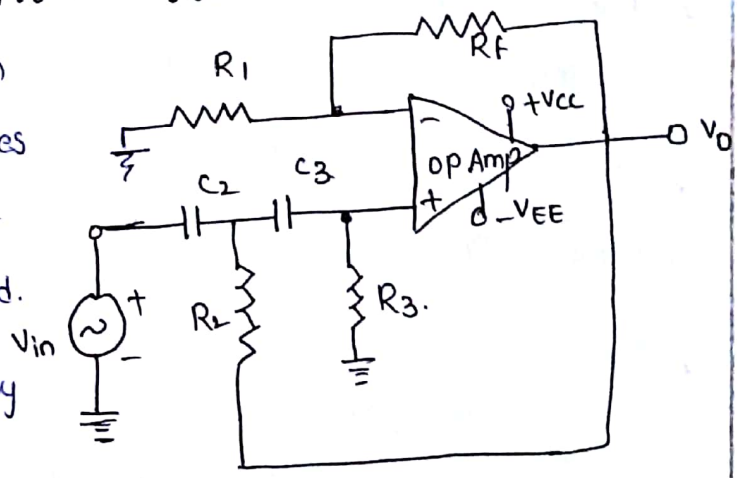
Hence slope is +20 dB/decade.



Second Order High pass Butterworth filter:

The second order High pass Butterworth filter produces a gain roll off at rate of 40 dB/decade in stop Band.

This can be obtained by interchanging of R and C in Second Order LPF.



The voltage Gain magnitude eqn for second order high pass filter is

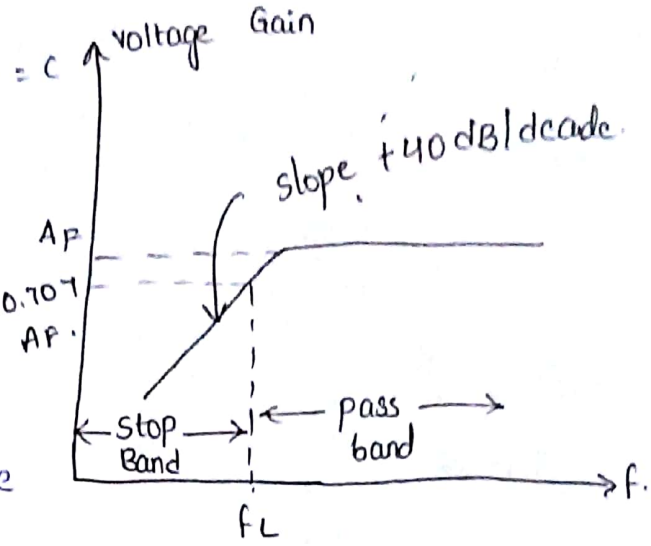
$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f_L/f)^4}} \quad \text{——— (1)}$$

Where f = I/p freq in Hz.

f_L = Lower cut off freq in Hz = $\frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$

If $R_2 = R_3 = R$ and $C_2 = C_3 = C$

then $f_L = \frac{1}{2\pi RC}$.



A_F = Pass band Gain

= 1.586 to ensure second order butterworth response

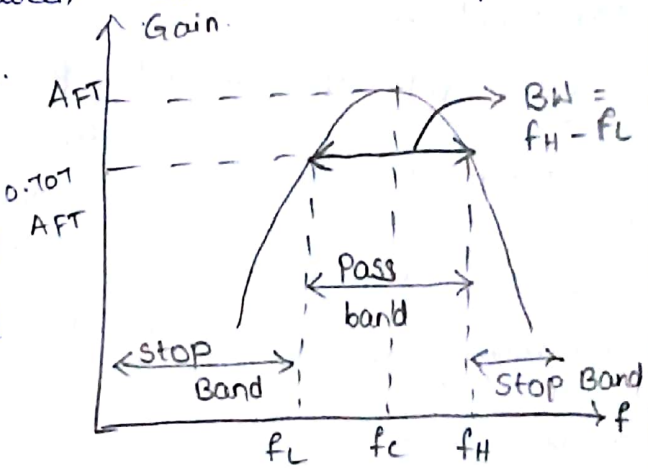
$R_F = 0.586\ R_1$

Band pass filter :

* The band pass filter basically a frequency Selector. It allows one particular band of frequencies to pass.

* Thus pass band is between two cut-off frequencies f_H and f_L where $f_H > f_L$.

* The pass band which is between f_H and f_L is called Band Width of filter denoted as B.W.



$$\boxed{BW = f_H - f_L} \quad \text{—(1)}$$

* The freq. at Centre of pass band is Centre freq. (f_c)

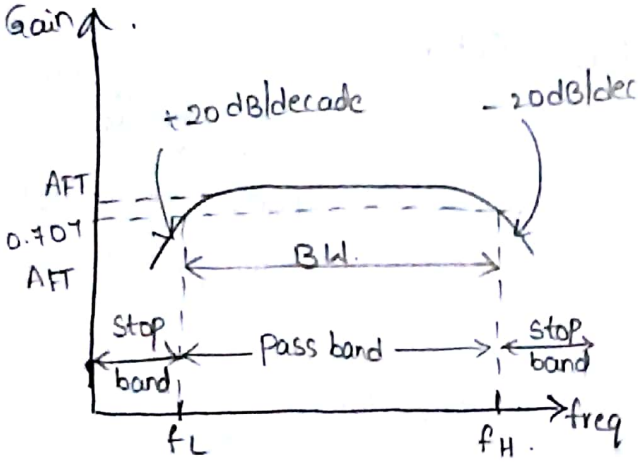
* The Gain is maximum at f_c and denoted as A_{FT} Called Total pass band Gain.

* There are two Types of Band pass filter which are classified based on "figure of Merit" (or) "Quality factor".

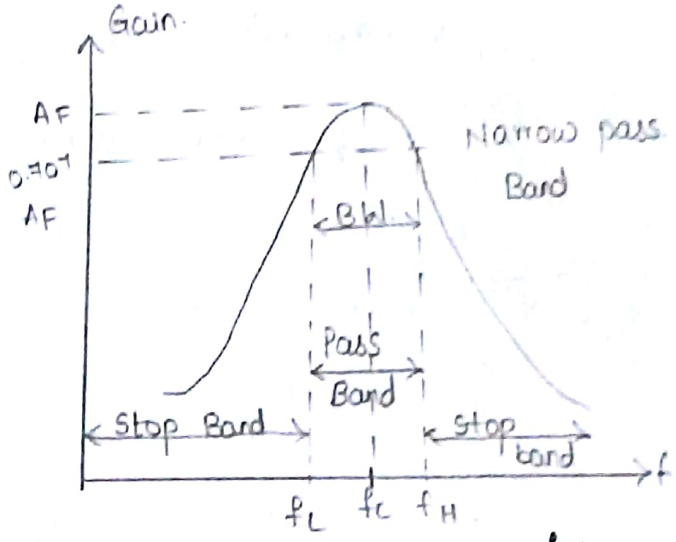
i) For $Q < 10$, the bandpass filter is called Wide Band pass filter. In this type, the bandpass is wide and and we get large BW. The Response is below (a)

ii) For $Q > 10$, the bandpass filter is called Narrow Band pass Filter. The band pass is very narrow and BW is very small. Higher value of Q, narrower is passband and more selective is the filter.

* The Gain roll off for $f < f_L$ is +20 dB/decade while $f > f_H$ is −20 dB/decade.



a) Wide band pass filter.



b) Narrow Band pass filter.

For wide band pass filter, the Centre freq is

$$f_c = \sqrt{f_L f_H} \quad \text{—— (2)}$$

The Relationship between Q and 3 dB BW with f_c is

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L} \quad \text{—— (3)}.$$

Wide Band pass filter:

The Wide band pass filter can be realised by simply Cascading high pass filter and LPF.

* If both high pass & low pass filter are of first order, the gain roll off in both stop bands are ±20 dB/decade. and Wide Band P.F is of 1st order.

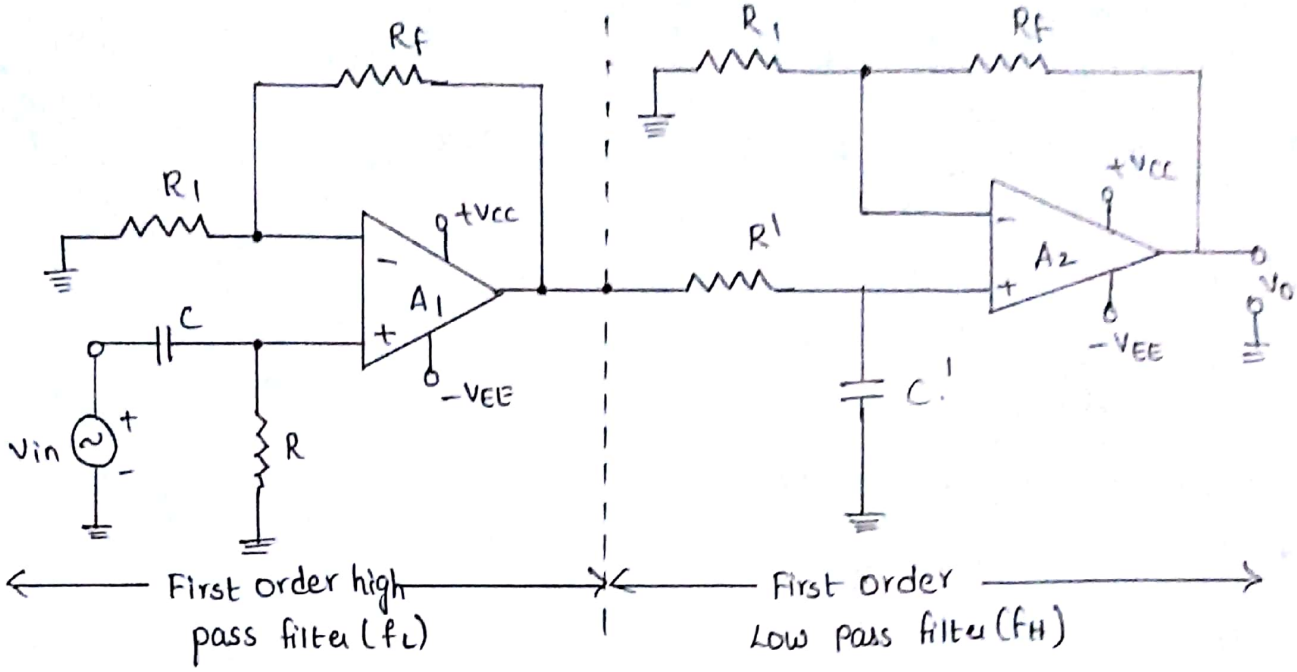


Fig: Wide Band Pass Filter.

For wide band pass Response, f_H must be greater than f_L. The voltage gain expression for two sections are reproduce here for convenince.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^2}} \quad \text{Low pass.}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\,(f/f_L)}{\sqrt{1+(f/f_L)^2}} \quad \text{High pass.}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}\,[f/f_L]}{\sqrt{[1+(f/f_L)^2]\,[1+(f/f_H)^2]}} \quad \text{——— (4)}$$

Where A_{FT} = Total pass band gain.

f = i/p frequency in Hz.

f_L = Lower Cut-off frequency in Hz.

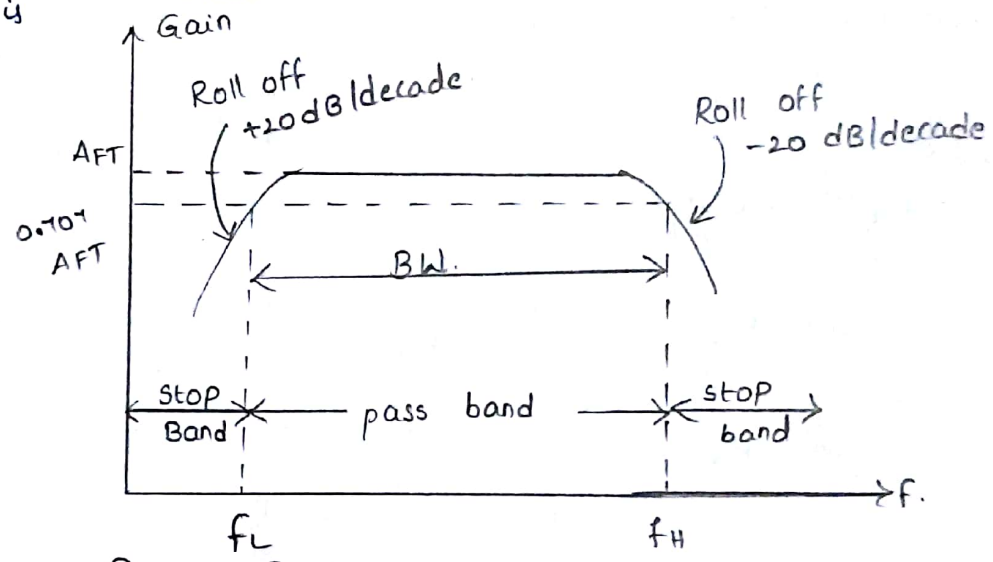
f_H = Higher Cut-OFF frequency in Hz

$$\boxed{A_{FT} = A_1 A_2} \quad \text{—— (5)}$$

Where A_1 = Gain of high pass section

A_2 = Gain of Low pass section.

* The frequency response such first order wide band pass filter is shown in fig below.

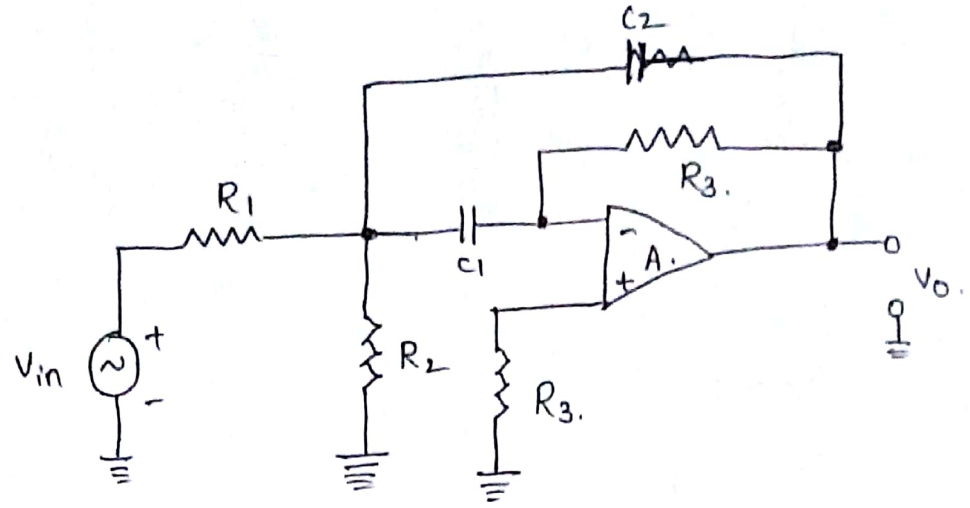


Narrow Band Pass Filter:

* The narrow band pass filter uses only one Op-Amp as aganist two by wide band pass filter. It has following features.

1. It has two feedback paths.
2. The OP-Amp is in the inverting Configuration.

* Due to two Feedbacks paths, it is called the Multiple Feedback filter.



* From the fig, the i/p applied to inverting i/p Terminal
Thus, OP-Amp is in Inverting Configuration. The R_3 connected
to non-inverting i/p terminal is offset compensating Res.

Note:

For Simplifying calculations choose $C_1 = C_2 = C$.

$$R_1 = \frac{Q}{2\pi f_c C A_F} \quad \text{——— (6)}$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)} \quad \text{——— (7)}$$

$$R_3 = Q / \pi f_c C \quad \text{——— (8)}$$

$$A_F = \frac{R_3}{2R_1} = \text{gain at } f_c \quad \text{——— (9)}$$

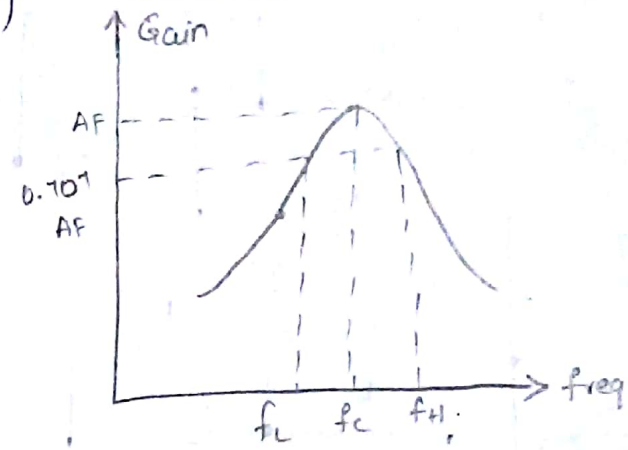
The gain A_F must satisfy eq^n $A_F < 2Q^2$ ——— (10).

Changing Centre freq (f_c):

Let f_c = Original freq.

f_c' = New centre frequency.

$$R_2' = R_2 \left(\frac{f_c}{f_c'}\right)^2 \quad \text{——— (ii)}$$



* This is important advantage of multiple feedback CKT, that f_c can be changed without changing Gain AF (or) Band Width

Band Elimination filter:

* This filter is also called as Band Stop filter (or) Band reject Filter. The Action of this filter is Exactly opposite to Band pass Filter.

* The Elimination filters are two Types.

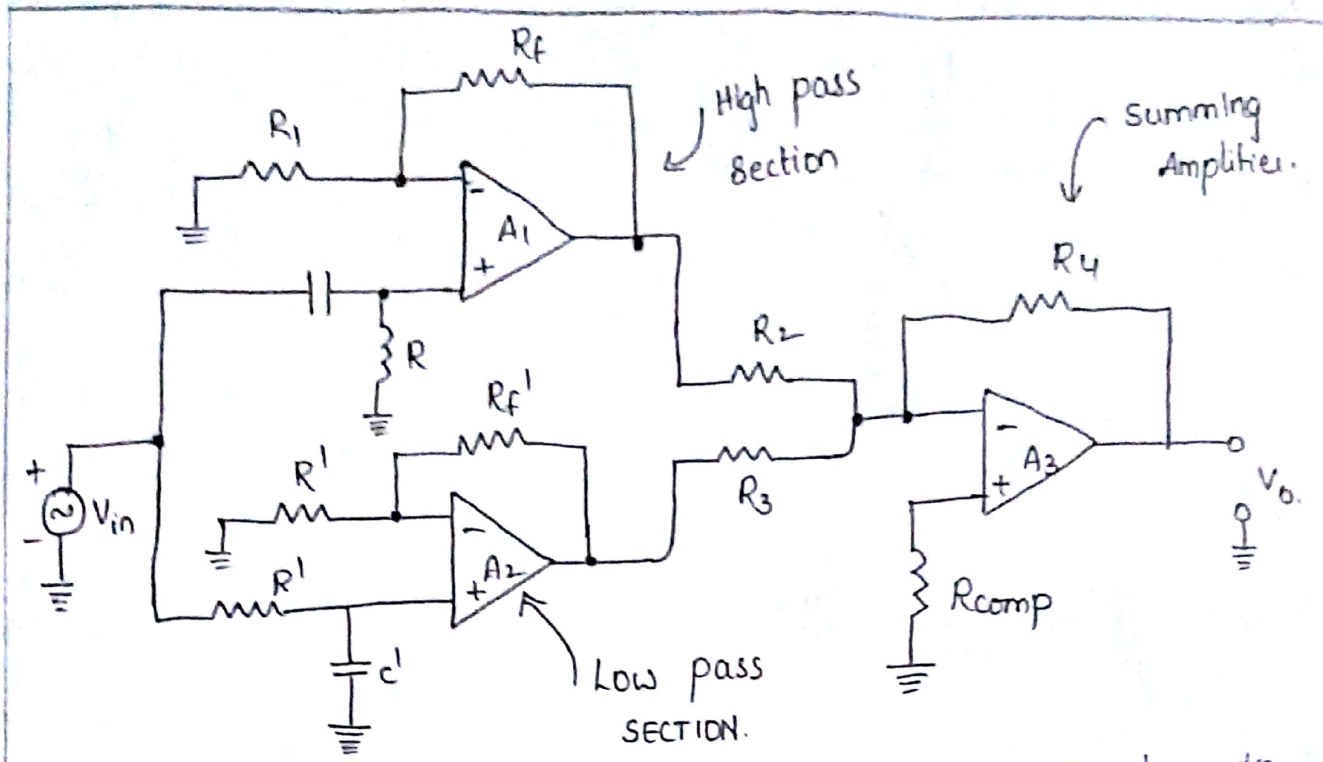
1. Wide Band Reject filter.
2. Narrow Band Reject filter.

* The FOM [Q] for narrow band filter is greater than 10. In its frequency response, it shows notch, hence Called as Notch filter.

* The BW of the Notch filter is very Small as Compared to Wide band Reject filter.

Wide Band Reject filter:

* Similar to Wide band pass filter, this filter also consists of high pass and low pass filter sections. Additionally, it consists of Summing amplifier.



The have satisfactory operation of filter, it has to satisfy following two conditions.

1. The low cut-off frequency, f_L of high pass filter must be greater than high cut-off freq, f_H of LPF.

The pass band gain of both high pass and low pass sections must be equal.

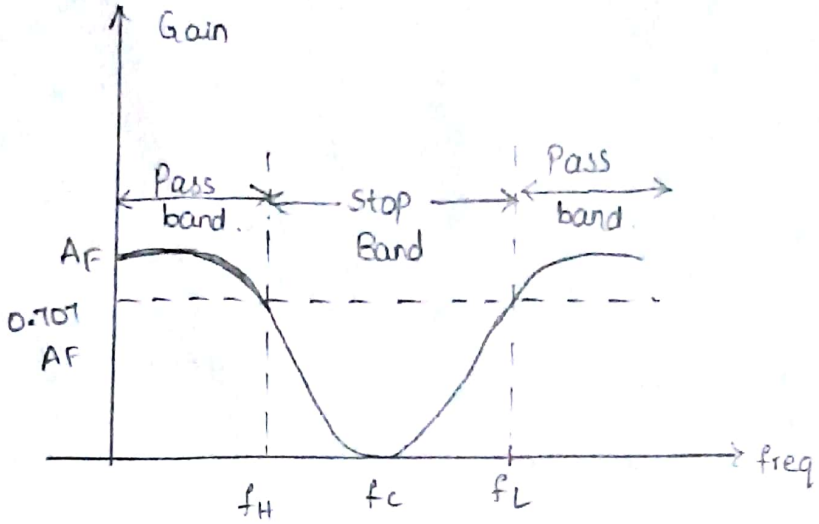
The design of overall filter is based on individual design of various section.

The gain of summing Amp can be set to 1 for simplicity and thus

$$R_2 = R_3 = R_4 = R \quad \text{—— (1)}$$

$$R_{comp} = R_2 \parallel R_3 \parallel R_4 = \frac{R}{3} \quad \text{—— (2)}.$$

Both high pass & Low pass sections provide attenuation in stop band between f_H and f_L. For $f < f_H$, is due to HPF. due to LPF, while for $f > f_L$ the



The Centre frequency, fc given by.

$$\boxed{f_c = \sqrt{f_H f_L}}$$

Narrow Band Reject filter [Notch filter]

* The name of filter i.e., Notch filter is due to its frequency Response Curve. The Characteristic shape of stop Band of filter is very narrow.

* The passive circuit used to obtain the notch filter is twin "T" Network as shown below.

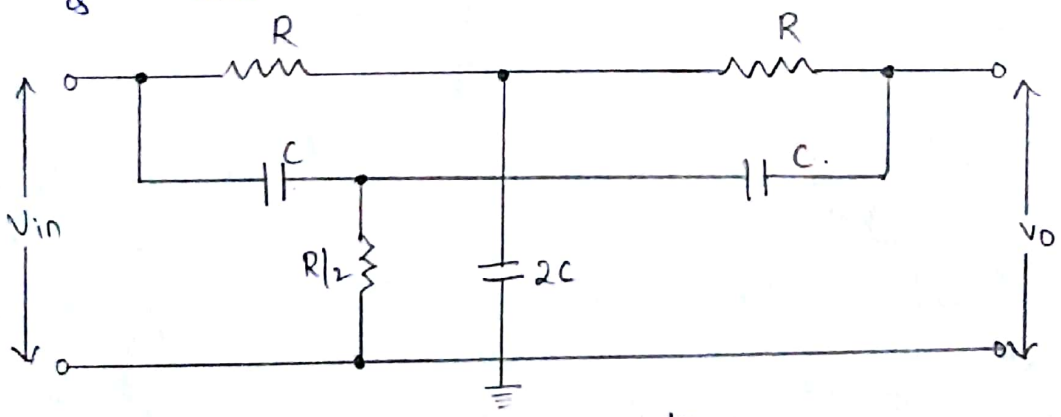


Fig: TWIN - T - Network

* It Consists of Two "T" Ntwoks. One Consists of 2 resistor and Capacitor while other Consists of two Capacitors and One resistor.

* The Notch out freq is freq at which max. attenuation occurs. This given by

$$f_N = \frac{1}{2\pi RC}$$

* The value of Q i.e., FOM for passive ntwk is very low, hence active notch filter which uses twin "T" Ntwk is preferred in practice.

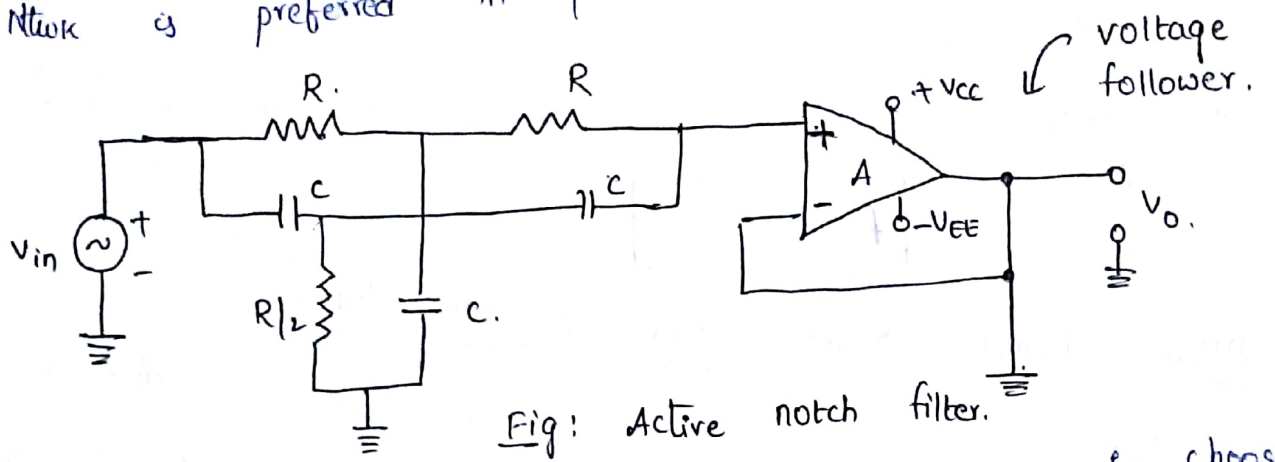
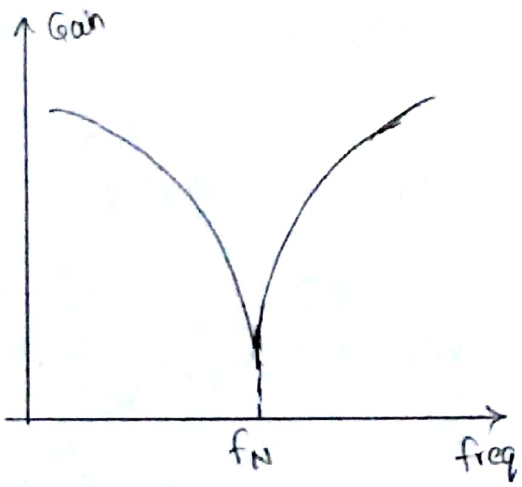
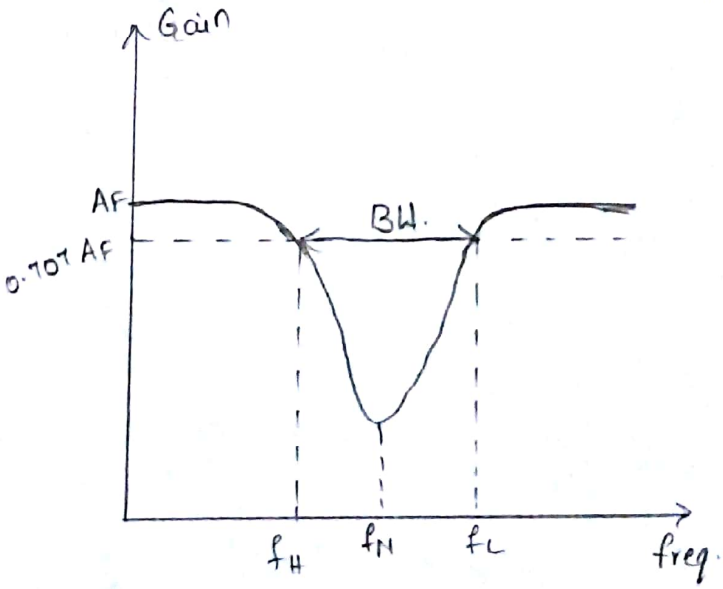


Fig: Active notch filter.

To Eliminate the specific notch frequency, f_N choose Capacitor "C" less than or Equal to 1μF. Then cal value of R using Eqn ③. The components designed should have precise filter.



(a) Ideal

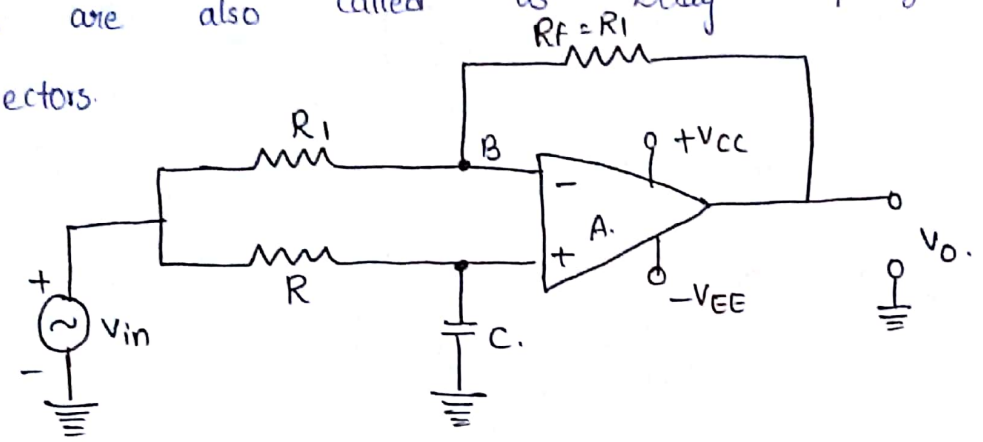


b) practical.

All Pass filter :

* When Signals are Transmitted over the Transmission lines, there is change in their phase. To compensate for such phase change, all pass filters are Used.

* Hence all pass filters are used. Hence all pass filters are also called as Delay equalizers / phase correctors.



Analysis :

* Let us see superposition principle to obtain Exp for o/p vltg (V_o). Assume i/p to non-inverting Terminal zero. The CKT acts as inverting Amp.

$$V_{o1} = -\frac{R_f}{R_1} V_{in}$$

$$V_{o1} = -V_{in} \quad (\because R_f = R_1) \quad \text{——— (1)}$$

* Assume i/p to inverting Terminal zero, CKT acts as Non-Inv

$$V_{o2} = \left(1 + \frac{R_f}{R_1}\right) V_A.$$

$$V_{o2} = 2 V_A \quad (\because R_f = R_1) \quad \text{——— (2)}$$

* By potential divider rule, V_A can be obtained

$$V_A = V_{in} \left[\frac{-jX_C}{R - jX_C}\right]$$

$$-jX_C = -j\left[1/2\pi fC\right] = \left(1/j2\pi fC\right) \quad \text{as } -j = 1/j$$

$$V_A = V_{in}\left[\frac{1/j2\pi fC}{R + 1/j2\pi fC}\right]$$

$$V_A = V_{in}\left[\frac{1}{1 + j2\pi fRC}\right] \quad \text{—— (3)}$$

Sub (3) in (2)

$$V_{o2} = 2\,V_{in}\left[\frac{1}{1 + j2\pi fRC}\right] \quad \text{—— (4)}$$

Hence total o/p vltg is

$$V_o = V_{o1} + V_{o2}$$

$$= -V_{in} + 2V_{in}\left[\frac{1}{1 + j2\pi fRC}\right]$$

$$= V_{in}\left[-1 + \frac{2}{1 + j2\pi fRC}\right]$$

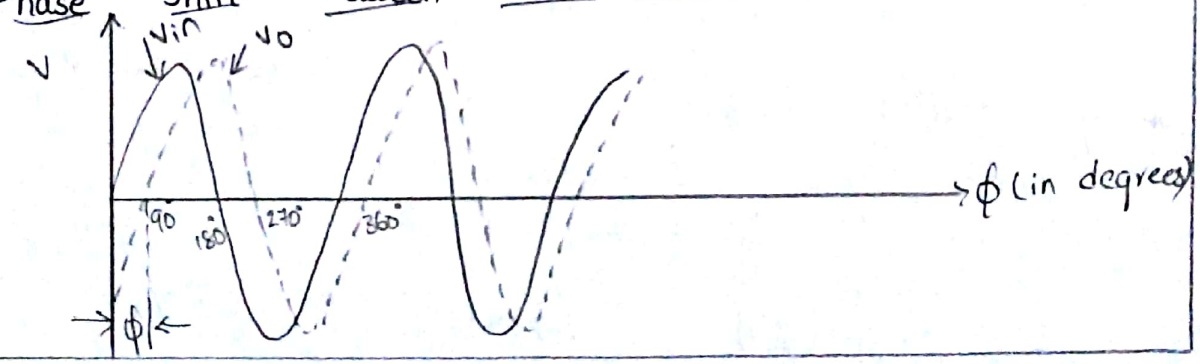
$$\frac{V_o}{V_{in}} = \frac{1 - j2\pi fRC}{1 + j2\pi fRC} \quad \text{—— (6)}$$

The Magnitude of T/F

$$\left|\frac{V_o}{V_{in}}\right| = \frac{\sqrt{1 + (2\pi fRC)^2}}{\sqrt{1 + (2\pi fRC)^2}} = 1. \quad \text{—— (7)}$$

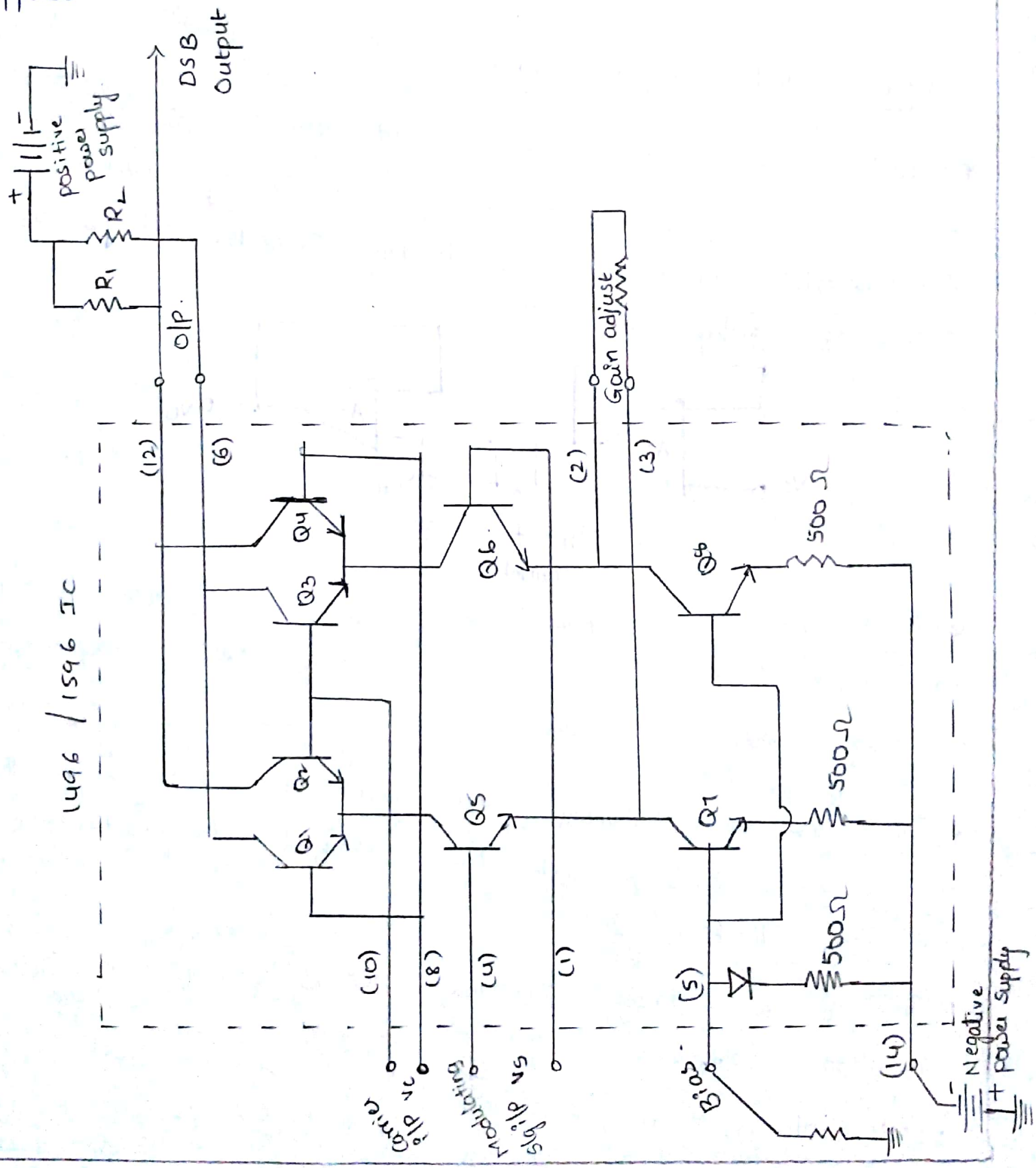
$$\phi = -2\tan^{-1}\left[\frac{2\pi fRC}{1}\right] \quad \text{—— (8)}$$

Fig: Phase shift between V_o and V_{in}.



Balanced Modulator (IC 1496)

* In this Transistor Q_7 & Q_8 are constant current sources. Q_1, Q_5, Q_2 from one differential Amp & Q_3, Q_4, Q_6 form another Diff. Amp. The constant current sources supply equal amount of current to 2 Diff. Amp. The carrier signal is applied in phase as biasing signal for Diff. Amp.

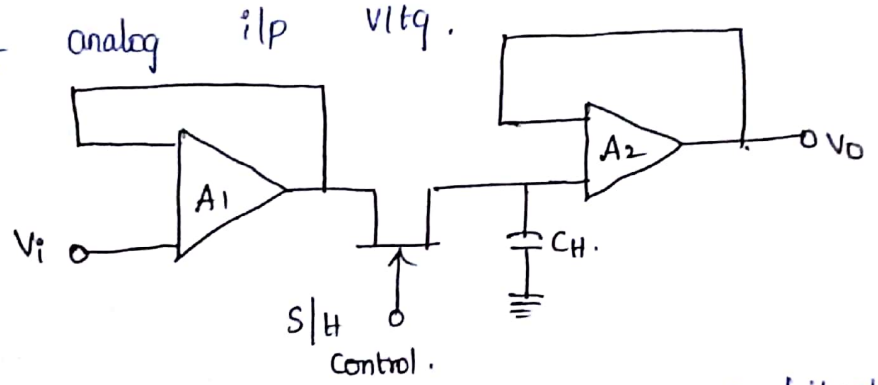


* The modulating signal applied to bases Q_5 and Q_6. These transistors are connected in current paths to differential Transistor, and therefore will vary Amplitude of current in accordance with modulating signal.

* The currents in Q_5 and Q_6 will be 180° out of phase with each other. As the current Q_5 (↑) current through Q_6 (↓) and vice versa.

Sample and Hold Circuits:

* Four basic sample and hold circuits as shown. In these JFET is used as switch. During sampling time JFET switch turned ON, the holding capacitor charges up to level of analog i/p vltg.



* The above fig, shows open loop architecture of sample and hold CKT. Remaining fig, shows closed loop architecture of sample and hold CKT.

* Open loop type sample and hold CKT are faster than closed loop types which have delayed o/p fed back to i/p buffer.

* There are three principle factors that will control acquisition time.

→ These factors are:

1. RC time Constant where R is r_{ds} (ON) i.e., ON Res of JFET and C is holding Capacitance (C_H)

2. Maximum o/p current, which can be source / sink by operational amplifier.

The change in voltage unit time applied

3. Slew Rate of Op-Amp.

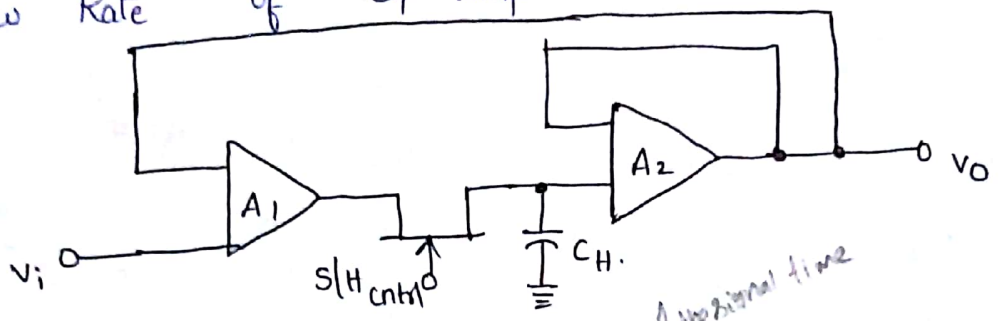


Fig (b)

The detection & the signal time

* The above fig offers some advantage over that fig (a) in terms of acquistion time since r_{ds} (ON) of JFET Switch is inside F/B of loop A_1 and A_2. It's acquisition Time is limited by max. o/p Current & Slew Rate rater than RC time constance.

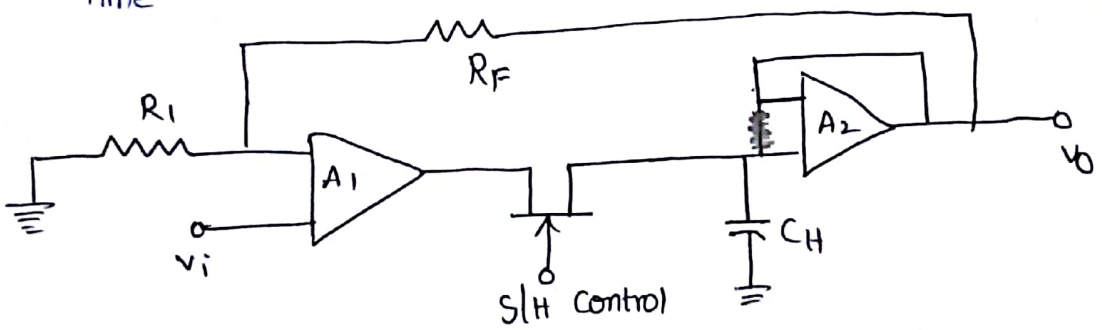


fig (c).

* The above fig performs in fashion similar to fib (b). but it offers additional fature of providing vltg gain. The vltg Gain of CKT $A = 1 + (R_F / R_1)$. Therefore, sampled o/p vltg Equal to sampled o/p vltg multiplied by vltg gain factor of $1 + \left(\frac{R_F}{R_1}\right)$.

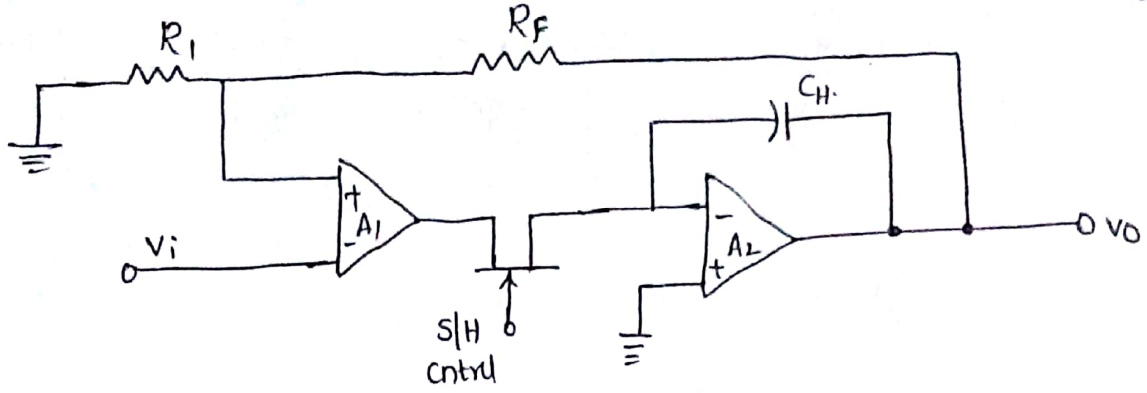
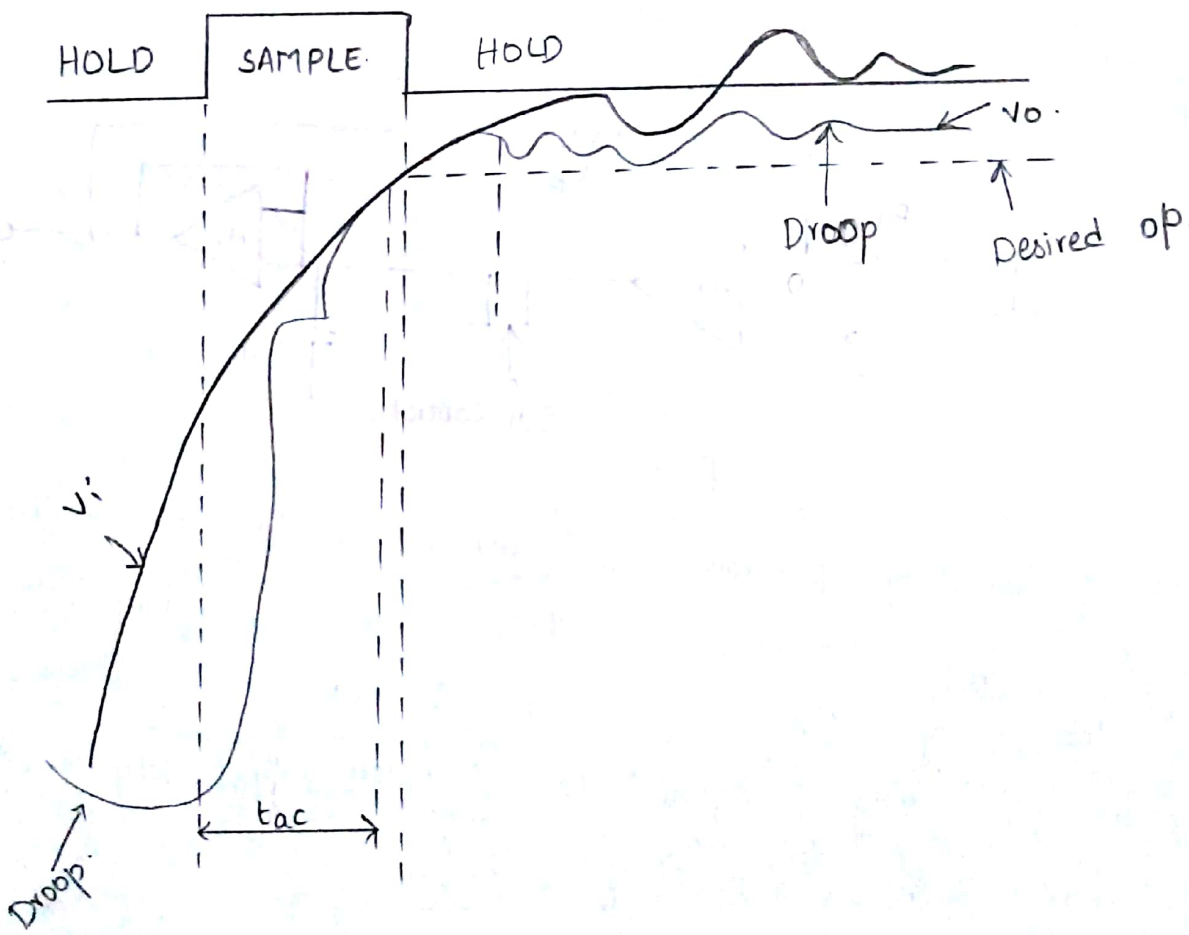


fig (d) :

* The above offer two Advantages. The faster Capacitor Charging rate provides shorter acquisition Time. This bcz vltg at inverting i/p terminal of A_2 equal to V_c divide open Loop gain of A_2.

Performance Parameters of S|H Circuits :



Acquisition Time (t_{ac}):

* It is time required for holding capacitor C_H to charge up to level close to i/p vltg during sampling. It depends on three factors.

1. RC time constant
2. Maximum Output Current of OP-Amp.
3. Slew rate of OP-Amp

Aperture Time (t_{ap}): Because of propagation delays through driver and Switch, V_o will keep tracking V_i, some time after inception of hold Command. This is aperture Time.

Aperture Uncertainity (Δt_{ap}): It is variation in aperture time from sample to sample. Due to aperture uncertainity it is difficult to compensate aperture time by advancing hold Command.

Holding mode Settling Time (t_s): After application of hold Command, it takes Certain amount of time for V_o to Settle within specified error band, such as 1%, 0.1%, 0.01%. This hold mode settling time.

Hold Step: Because of parasitic switch capacitance at Time of Switching between sample to hold mode, there is unwanted T/F of charge btw Switch driver and C_H. This Changes Capacitor vltgs & hence o/p vltg. This changes o/p vltg are referred to as hold step, pedestal

error and Sample to hold OFFset.

$$\Delta V_o = \frac{\Delta Q}{C_H} \quad \text{——— (1)}$$

Feedthrough :

* In the hold mode, bcz of Stray Capacitance across Switch, there is Small amount of a.c coupling between V_o and V_i. This ac Coupling Causes o/p vltg to vary with variation in i/p vltg. This is refered to as feed through and it given as

$$\Delta V_o \cong \frac{C_{ds}}{C_H} \Delta V_i \quad \text{——— (2)}$$

* Where C_{ds} is Stray Capacitance btw drain & Source JFET.

→ Feedthrough is usually Expressed in terms of feedthrough rejection Ratio (FRR) given as

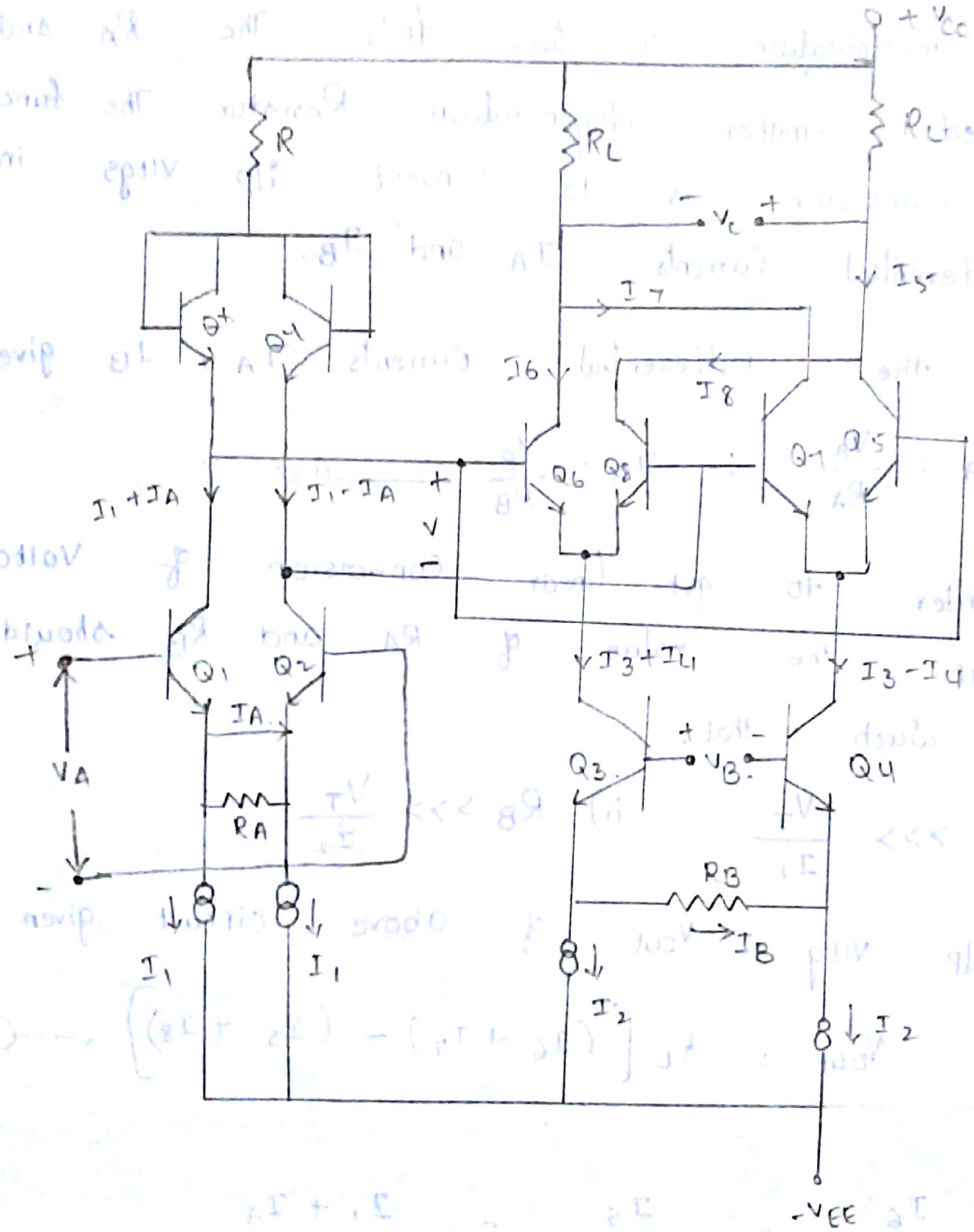
$$FRR = 20 \log_{10} \frac{\Delta V_i}{\Delta V_o}.$$

Applications :

1. Digital Interfacing.
2. Analog to Digital Converter CKT
3. pulse modulation System.
4. In Reset – stabilised Op-Amps
5. In Analog demux.
6. In Storage of o/p of mux btw updates in data distribution system.

Write Short Note on four Quadrant Multiplier.

* A circuit that functions in all four quadrant of operations and generates the product of two i/p voltages irrespective of polarity of its i/p signals is referred as four quadrant multiplier. It is designed in Monolithic form. Schematic Arrangement of four quadrant multiplier is illustrated below.



* When voltage V_A is applied as i/p to CKT and processed which then result in generation of intermediate voltages V across Q_x and Q_y. Any non-linearity Signal involved within V_A in generating V is inverse of non-linearity related with base emitter junctions of $Q_5 - Q_6$ and $Q_7 - Q_8$.

* Therefore, o/p voltage V_{out} of CKT is proportional to linear multiplication of two i/p's. The R_A and R_B are called emitter degeneration Resistor. The function of these resistor is to convert i/p vltgs into linear differential Currents I_A and I_B.

* Thus, the Differential Currents I_A, I_B given by

$$I_A = \frac{V_A}{R_A} \quad ; \quad I_B = \frac{V_B}{R_B} \quad \text{——} (1)$$

* In order to get linear Conversion of Voltage to Current, the value of R_A and R_B should be Selected Such that.

i) $R_A >>> \frac{V_T}{I_1}$ ii) $R_B >>> \frac{V_T}{I_2}$

* The o/p vltg, V_{out} of above circuit given by.

$$V_{out} = R_L \left[(I_6 + I_7) - (I_5 + I_8) \right] \quad \text{——} (2)$$

And

$$\frac{I_6}{I_3 + I_B} = \frac{I_5}{I_3 - I_B} = \frac{I_1 + I_A}{2 I_1}$$

$$I_6 = (I_3 + I_B)(I_1 + I_A) / 2 I_1 \quad \text{——} (3)$$

And Also

$$\frac{I_8}{I_3 + I_B} = \frac{I_7}{I_3 - I_B} = \frac{I_1 - I_A}{2 I_1}$$

$$I_8 = \frac{(I_3 + I_B)\ (I_1 + I_A)}{2 I_1} \quad \text{—— (5)}$$

$$I_7 = \frac{(I_3 - I_B)\ (I_1 - I_A)}{2 I_1} \quad \text{—— (6)}$$

$$I_5 = \frac{(I_3 - I_B)\ (I_1 + I_A)}{2 I_1} \quad \text{—— (4)}$$

By substituting eq^n (3), (4), (5) and (6) in (2) we get

$$V_{out} = R_L \left[\frac{I_1 I_3 + I_3 I_A + I_1 I_B + I_A I_B + I_1 I_3 - I_3 I_A - I_1 I_B + I_A I_B}{2 I_1} \right]$$

$$- \left(\frac{I_1 I_3 + I_3 I_A - I_1 I_B - I_A I_B + I_1 I_3 - I_3 I_A + I_1 I_B - I_A I_B}{2 I_1} \right)$$

$$= R_L \left[\frac{4 I_A I_B}{2 I_1} \right]$$

$$V_{out} = 2 R_L \left[\frac{I_A I_B}{I_1} \right]$$

As I_A and I_B linearly proportional to V_A and V_B by using eq^n (1) V_{out} Can be Written

$$V_{out} = K \cdot V_A \cdot V_B$$

Where $k = \dfrac{2R_L}{J_1 (R_A R_B)}$

usually, 'k' value is choosen as 0.1f.

UNIT - V

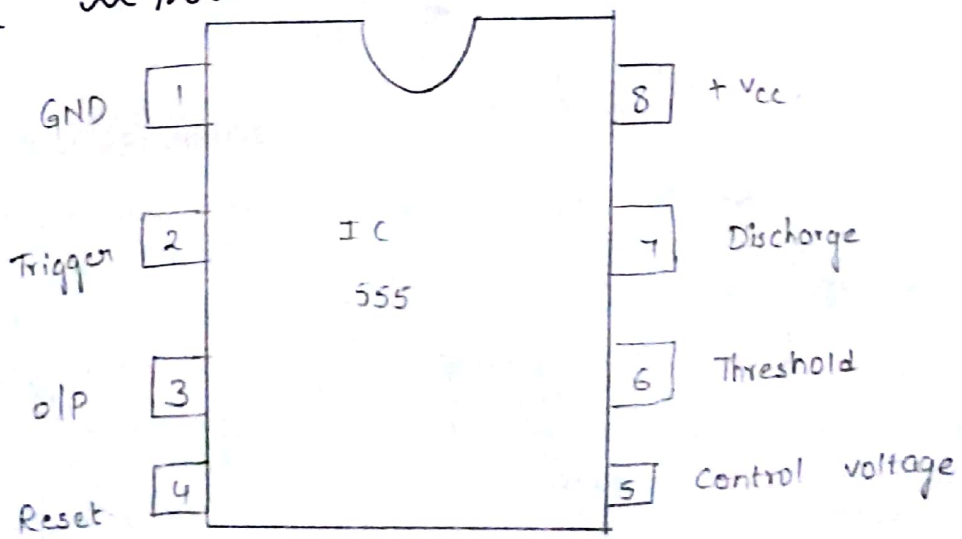
TIMERS AND PHASE LOCKED Loops:

Introduction to 555 timer:

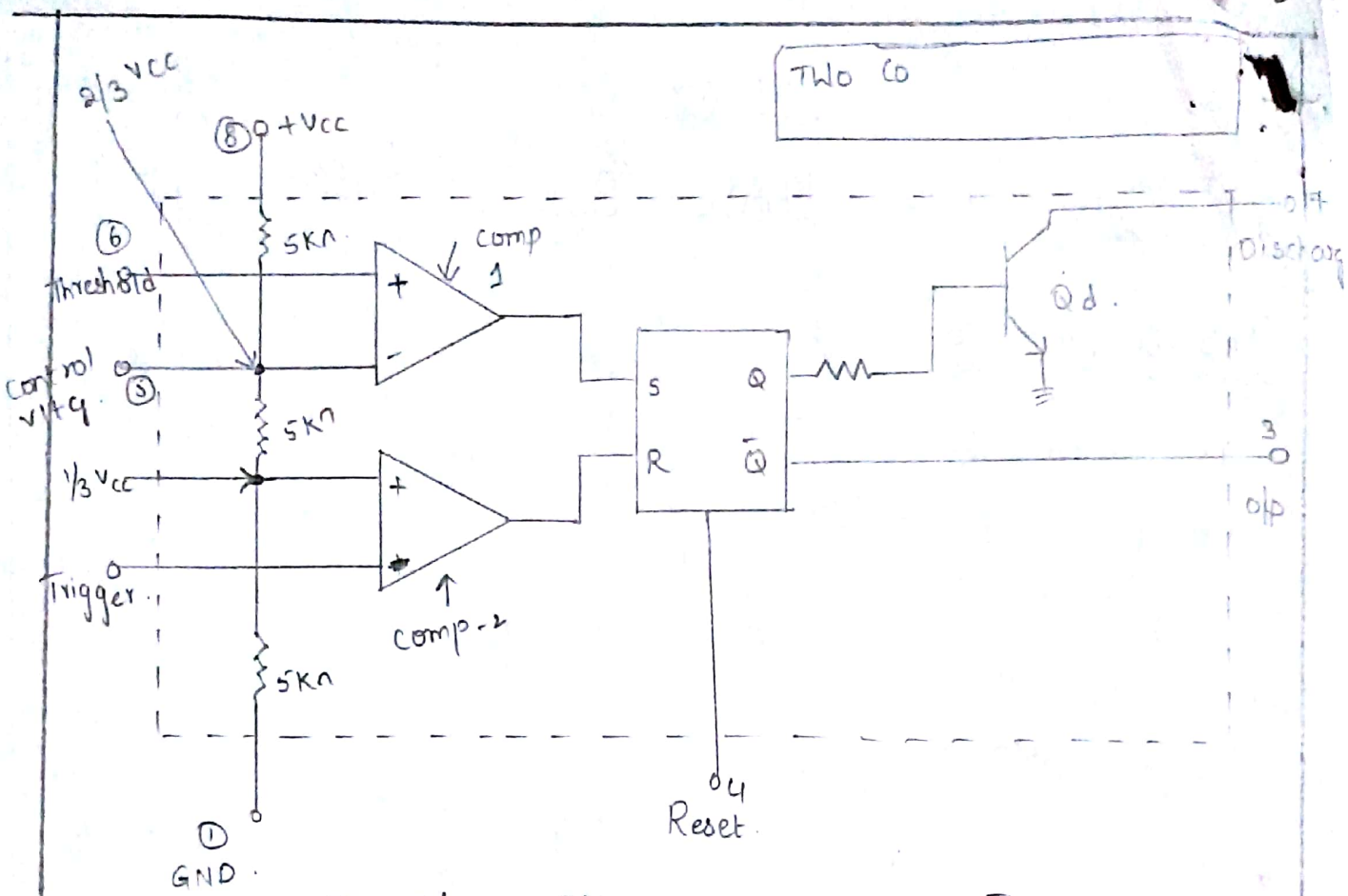
* In most of industries, operations are scheduled according to specific time requirements. In process Industry, raw material is proposed in different stages. In each stage raw material is processed for particular Time period.

* For Example, processor may be heating process and heat may be required to be applied for 5 minutes. There are no. of applications where event must be delayed for specific delay periods.

Functional Diagram:

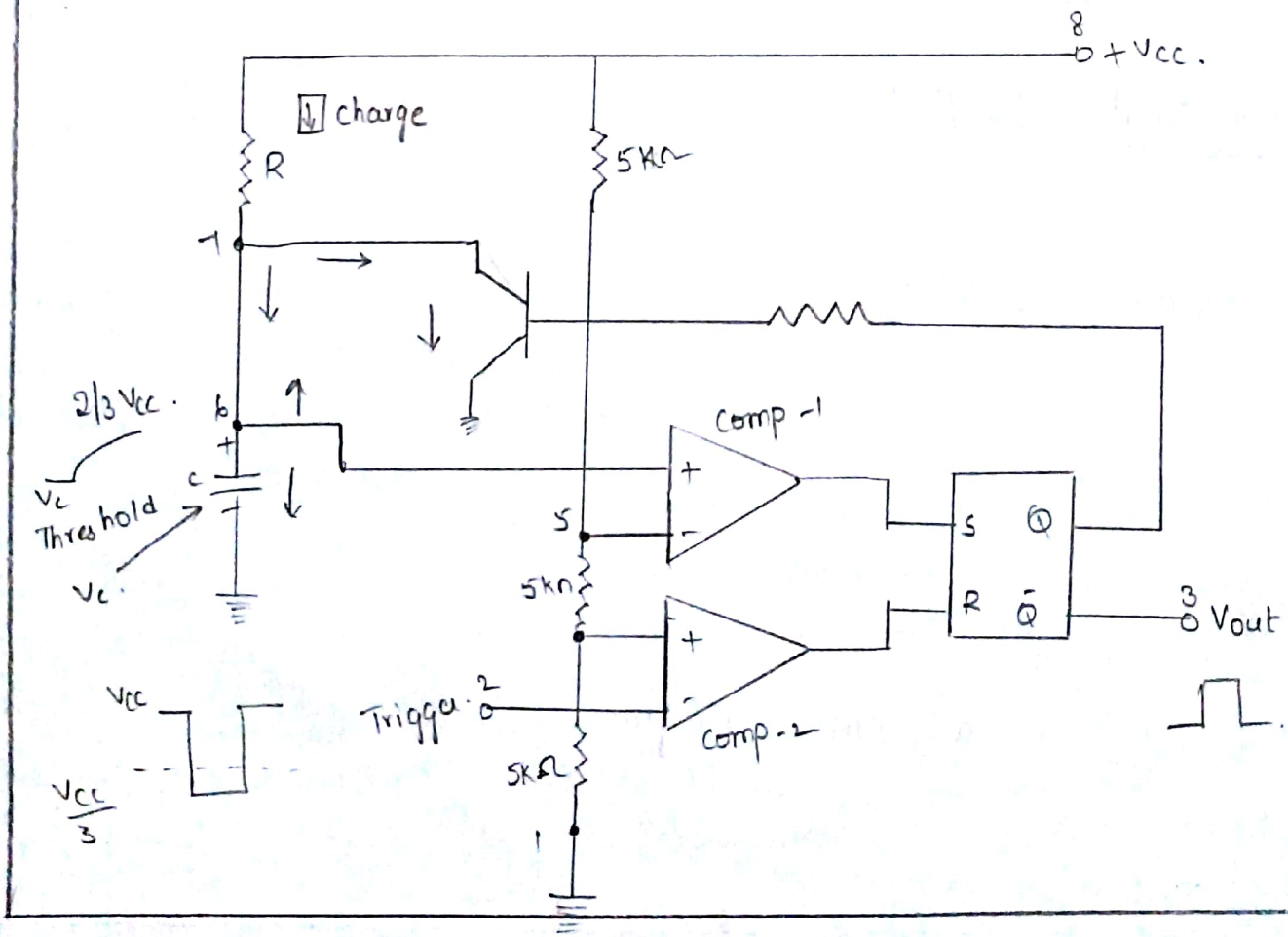


a) PIN Diagram.



Fig' Block Diagram of IC 555 Timer.

Monostable Multivibrator Using IC 555 :



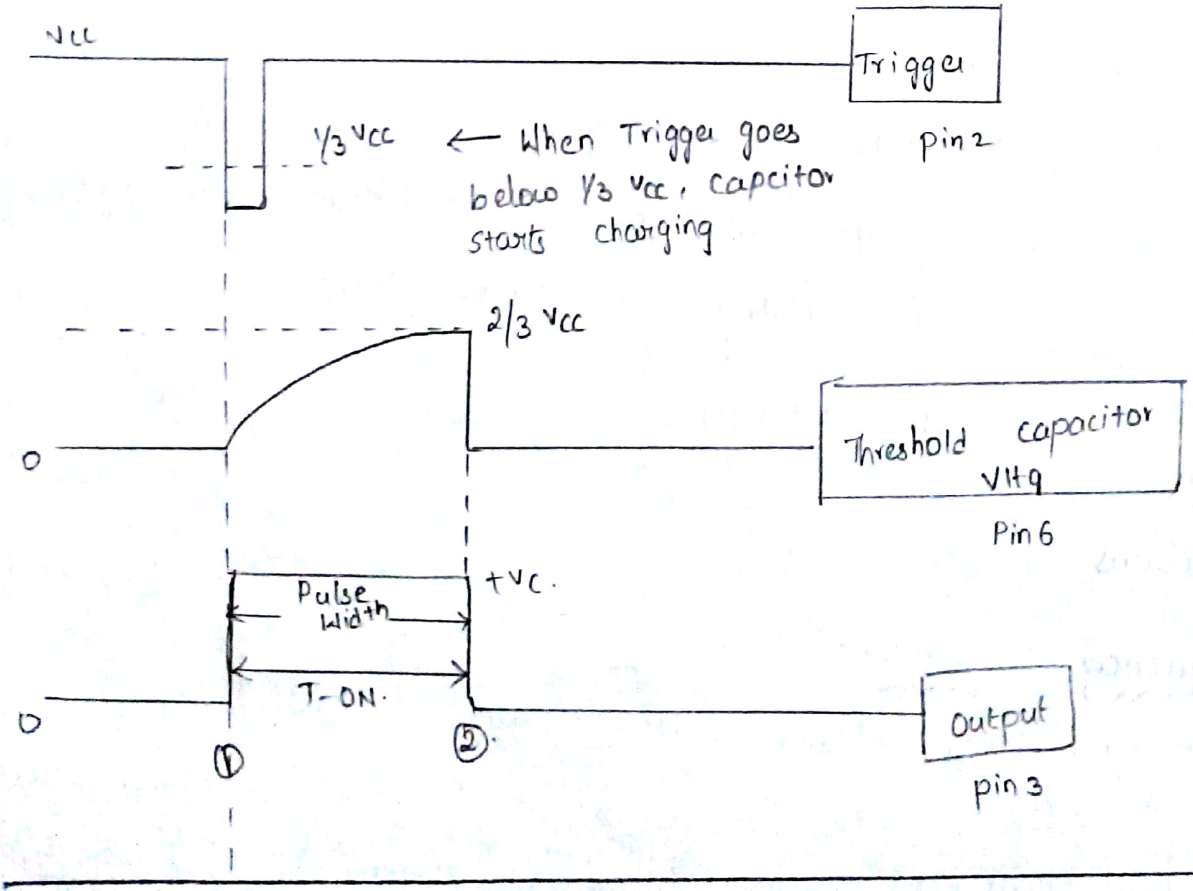
The IC 555 timer can be operated as Monostable multivibrator by connecting an external resistor and capacitor as show above.

Operation:

* The flip flop is initially set i.e., Q is high This drives Qd in Saturation The Capacitor discharges completely and voltage across it near by zero. The o/p at pin 3 low.

When Trigger i/p a voltage low going pulse applied, then ckt state remaining unchanged till trigger vltg is greater than 1/3 Vcc. When it becomes less than 1/3 Vcc, then comp - 2 o/p goes high.

This reset flip flop so Q goes low, $\bar{Q}$ goes high Low Q - makes transistor Qd OFF. Hence capacitor starts charging through R.



The Rectangular wave produced by o/p and the pulse width of rectangular pulse controlled by charging time of capacitor. This depends on time constant RC. Thus RC controls pulse width. The waveforms shown abov.

Derivation of pulse width:

The voltage across capacitor increases exponentially

$$V_c = V(1-e^{-t/RC})$$

$$V_c = 2/3\ V_{cc}$$

$$\frac{2}{3} V_{cc} = V_{cc}(1-e^{-t/RC})$$

$$\frac{2}{3} - 1 = -e^{-t/RC}$$

$$-t/CR = -1.0986.$$

$$t = 1.1\ CR.$$

Where $c \rightarrow$ Farads $R \rightarrow$ ohms $t \rightarrow$ in seconds.

Thus we can say vltg across capacitor will reach 2/3 V_{cc} in approximately 1.1 times RC.

$$\boxed{W = 1.1\ RC}$$

Applications:

1. Frequency Divider:

W.K.T in monostable multivibrator, application of Trigger pulse give +ve going pulse on o/p. The same ckt can be used as freq. divider if timing interval adjusted

to be longer than period of i/p signal.

The below fig, shows monostable multivibrator as divider by 2 - CKT.

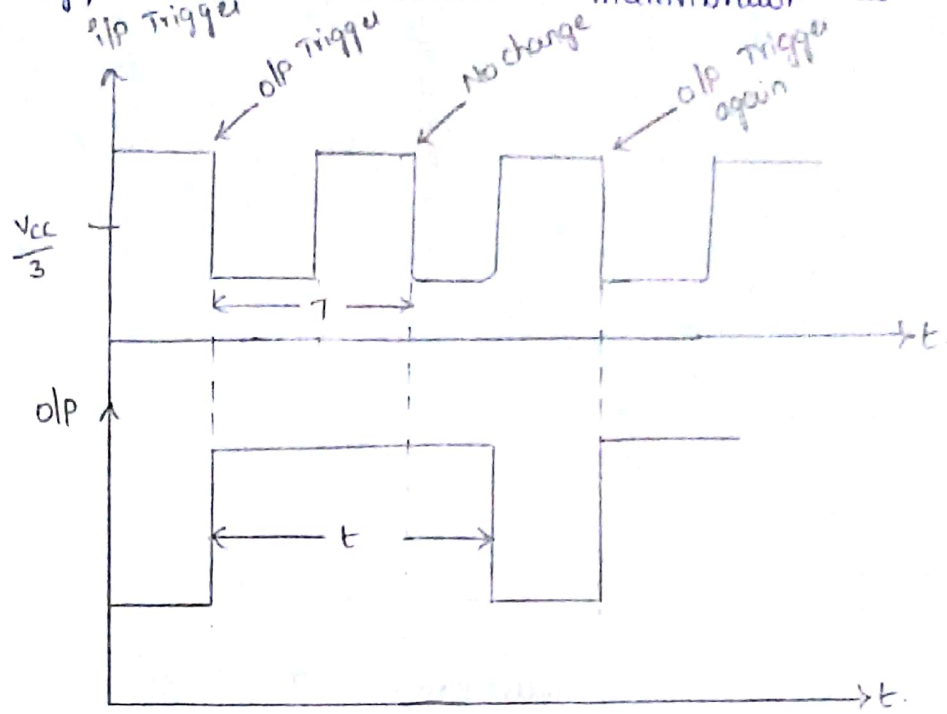
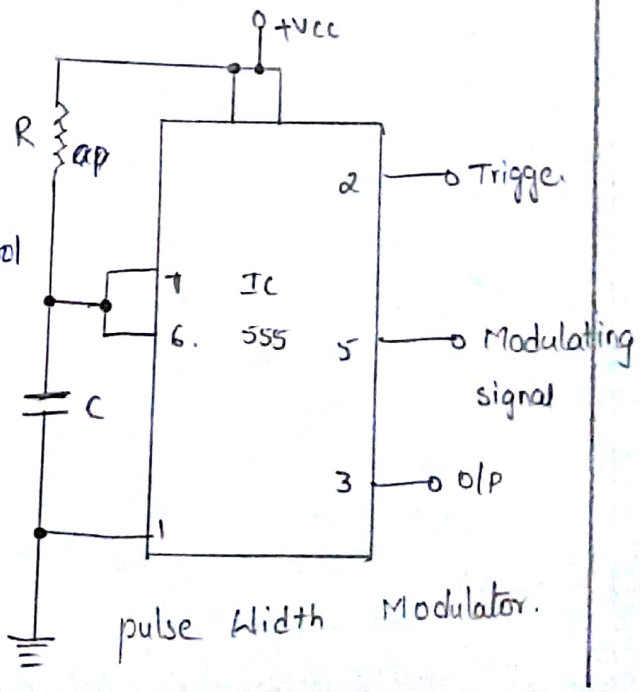


Fig: Input - Output Waveforms of monostable multivibrator as divide by 2 circuit.

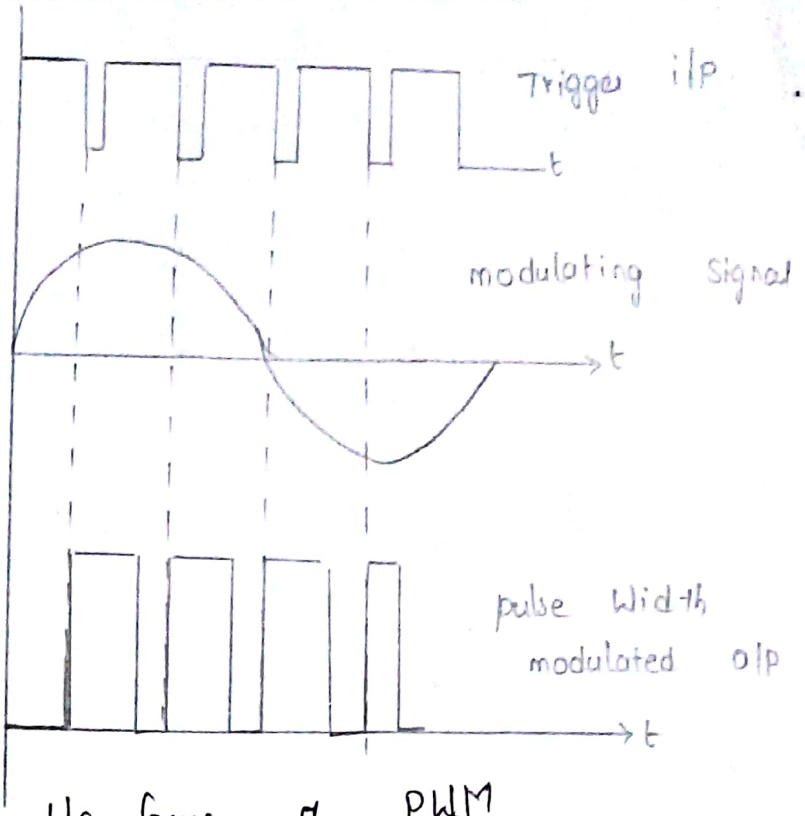
2. Pulse Width Modulation:

The below fig shows pulse Width Modulato. It is basically monostable multivibrator with modulating i/p signal applied at control voltage (Pin 5).

Internally, control voltage adjusted to the 2/3 Vcc. Externally applied modulating signal changes control voltage and hence threshold voltage level of Upper Comparator. As a result time period required to charge Capacitor upto threshold voltage level changes.



pulse Width Modulator.



Waveforms of PWM

3. Linear Ramp Generator :

When capacitor is charged with constant current source then linear ramp is obtained. This concept used in linear Ramp Generator. This CKT shown below.

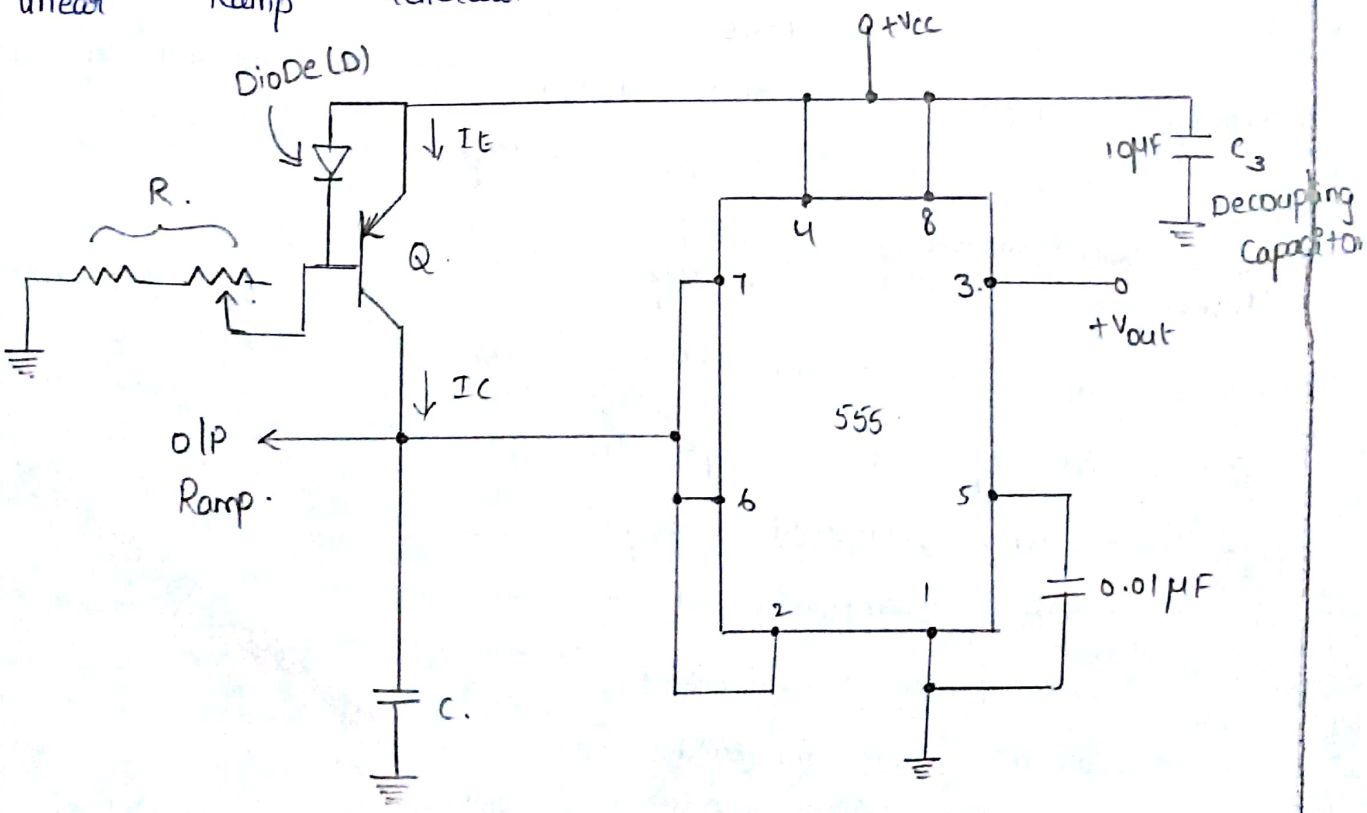


Fig: Linear Ramp Generator

* The CKT is used to obtain constant current I_c is current mirror CKT, using Q and D. The I_c charges capacitor "C" at constant rate towards $+V_{cc}$.

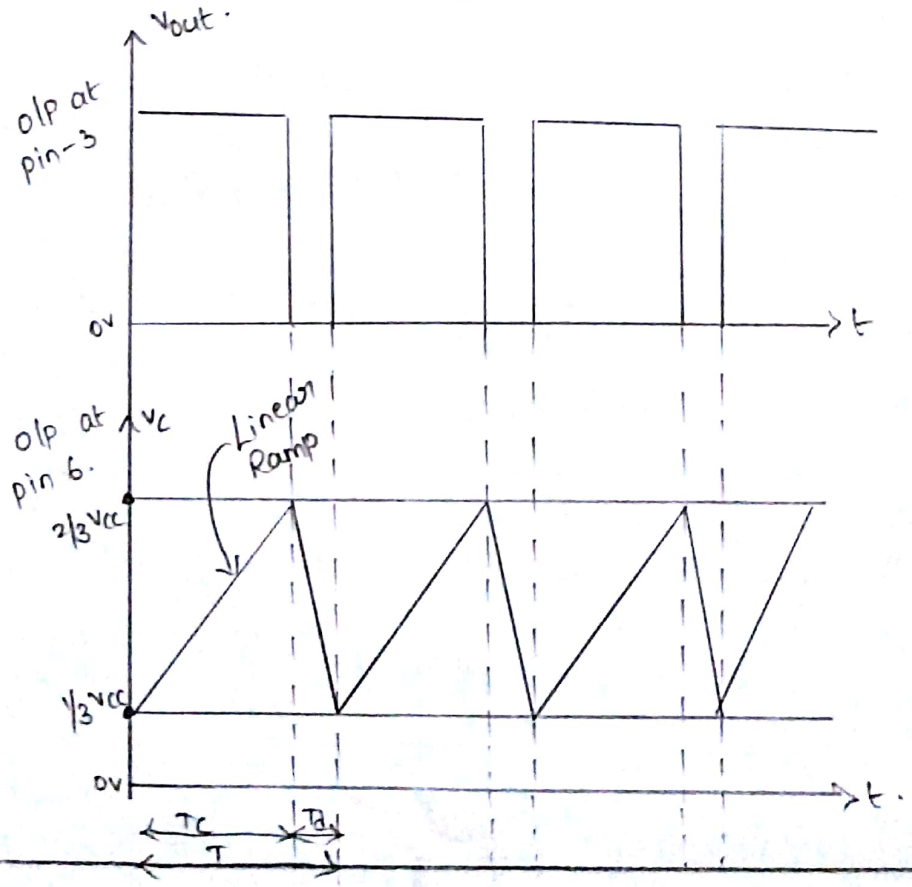
* But when voltage at pin 6 i.e., capacitor voltage becomes $(2/3\ V_{cc})$, comparator makes internal Q_1 ON within no time. But while discharging V_c becomes $1/3\ V_{cc}$.

* Second comparator Q_1 OFF; C starts it charging again. As discharging time of capacitor is very small, Time period of ramp assumed practically same as that of charging time of capacitor.

$$T = \frac{V_{cc}\ C}{3\ I_c}\ \text{sec.}$$

Where I_c = charging current $= \frac{V_{cc} - V_D}{R} = \frac{V_{cc} - V_{BE}}{R}$.

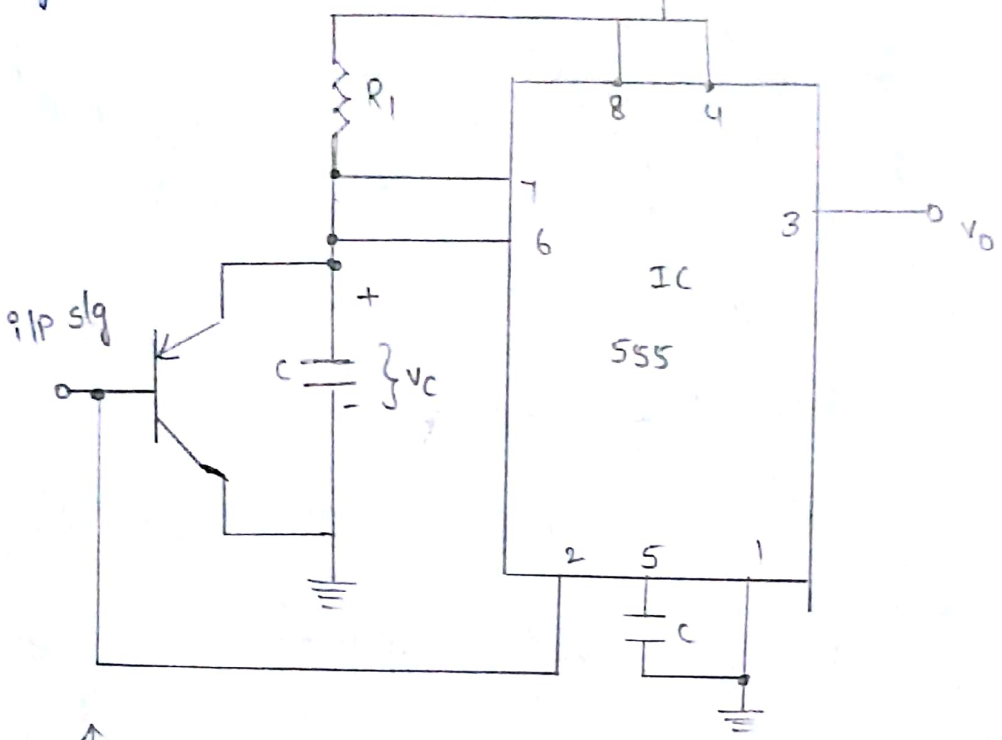
$$f = \frac{1}{T} = \frac{3 I_c}{V_{cc} \cdot C}\ \text{Hz.}$$

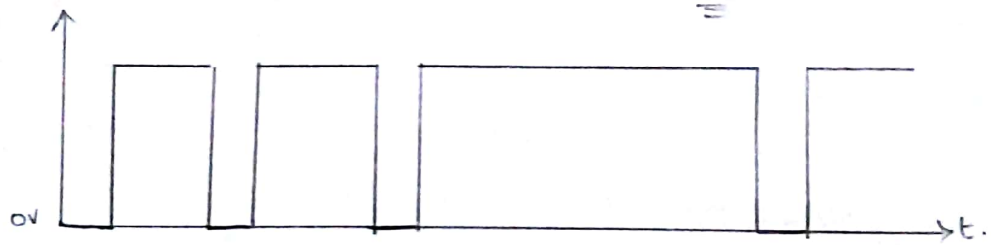


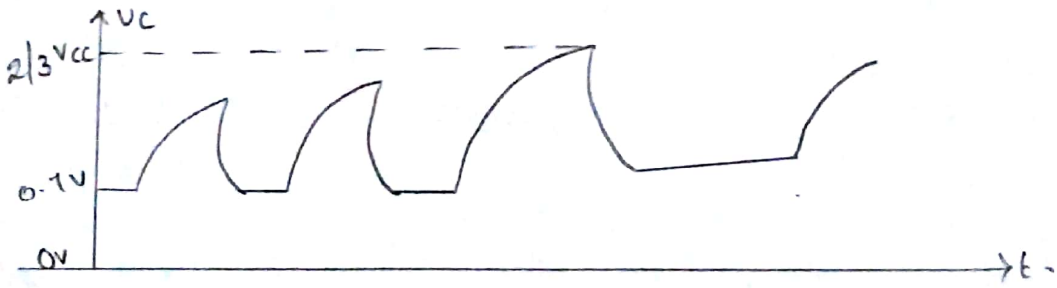
4. Missing pulse Detector:

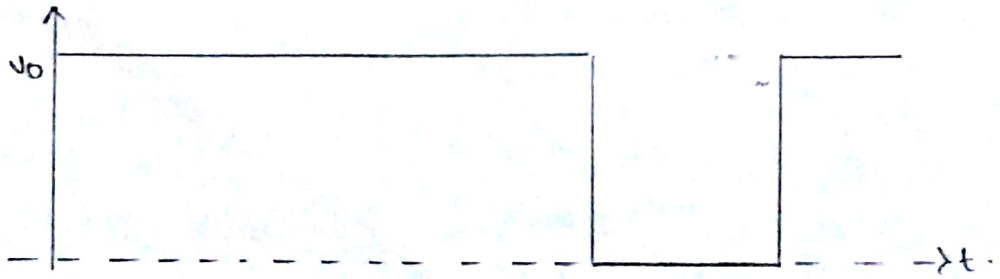
The below fig shows CKT diagram for missing pulse detector. When s/g i/p is at GND level (0V), the Emitter diode of T_1 f/B and clamps capacitor voltage (V_c) to 0.7V.

If i/p s/g again goes low before 555 completes its timing cycle, total voltage across C is reset 0.7V.



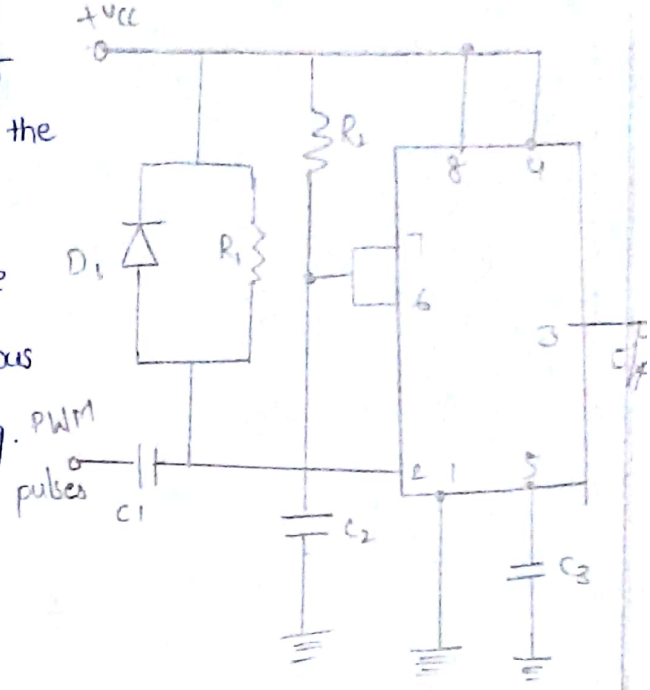


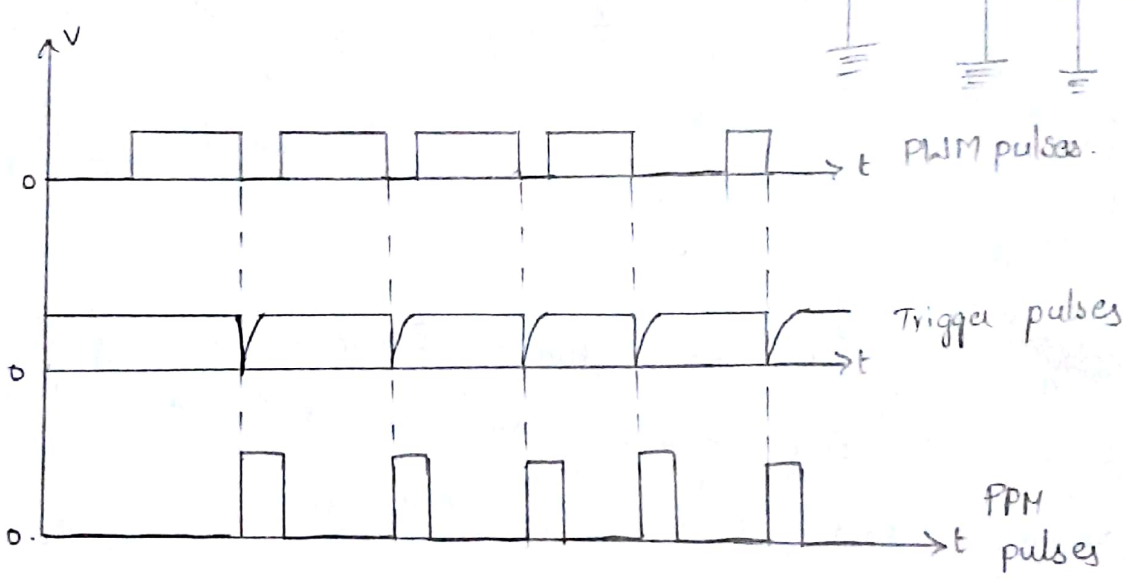




5. Pulse Position Modulation (PPM)

* In PPM, amplitude & width of pulses are kept constant, while the position of the each pulse with ref to position of reference pulse is changed according to instantaneous sampled value of modulating sig.





* The ckt diagram consists of Differentiator & monostable multivibrator. The i/p to differentiator is PWM waveform. The diff. generates +ve & -ve spikes corresponding to leading & travelling edges of PWM waveform.

Astable Multivibrator:

* The fig, shows IC 555 connected as an astable multi vibrator. The threshold i/p connected to trigger i/p. Two external resistance R_A, R_B and capacitor (C) is used in ckt

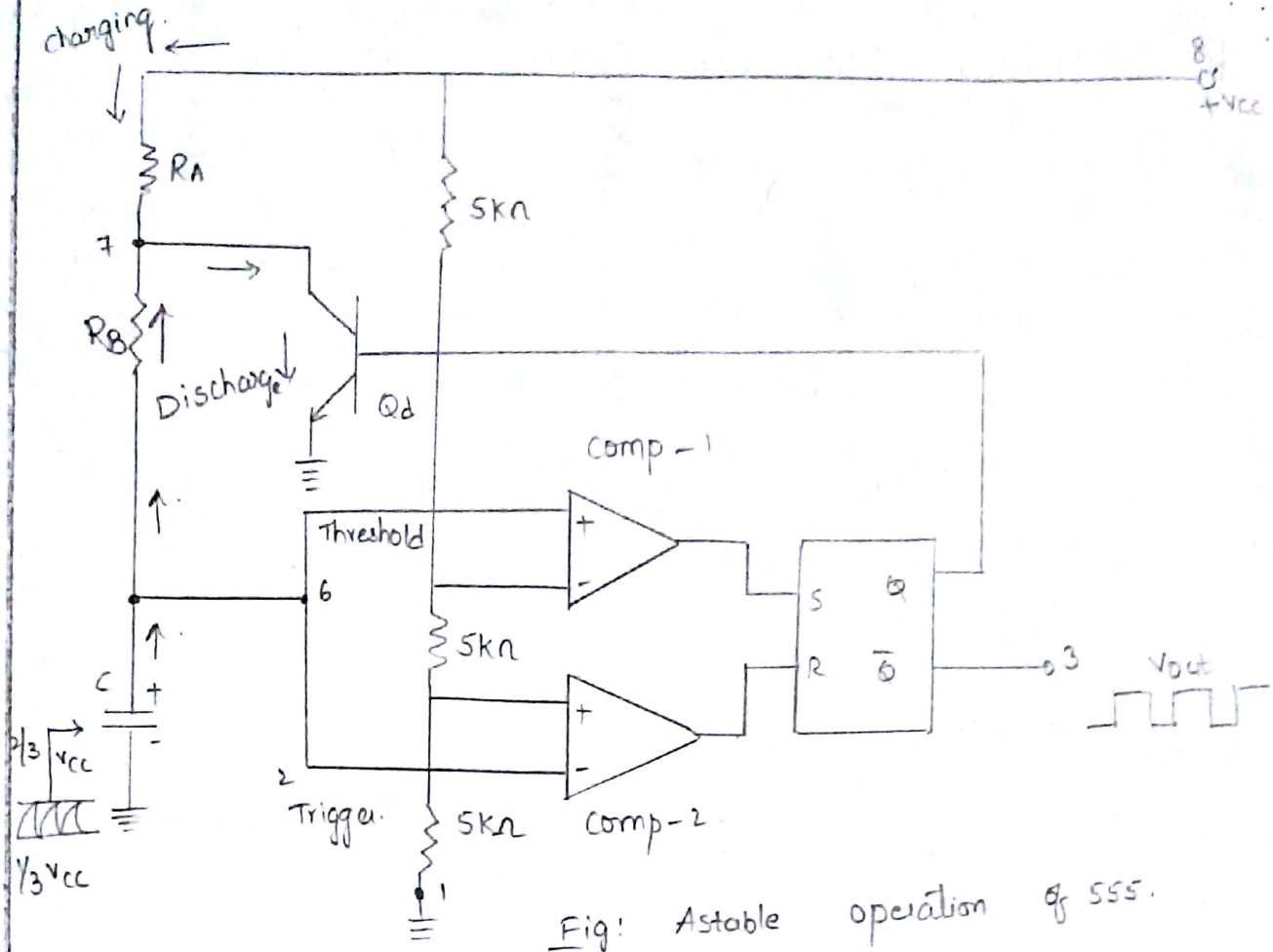
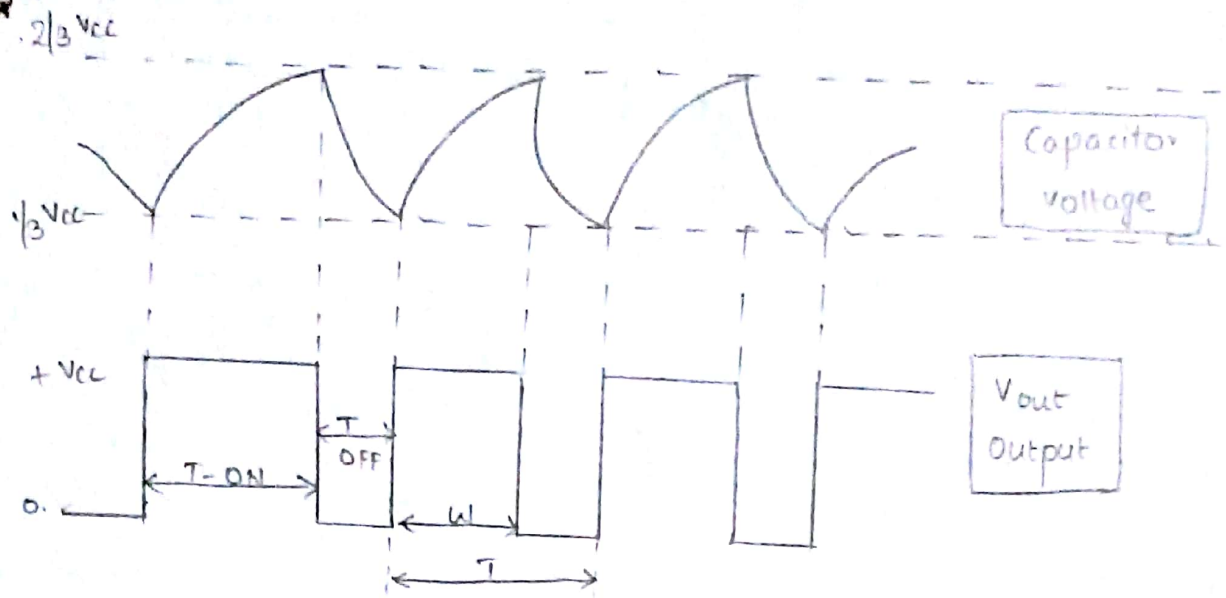


Fig: Astable operation of 555.

The CKT has no stable state. The CKT's changes its state alternately. Hence operation is also called free Running Non-sinusoidal Oscillator.

Operation :

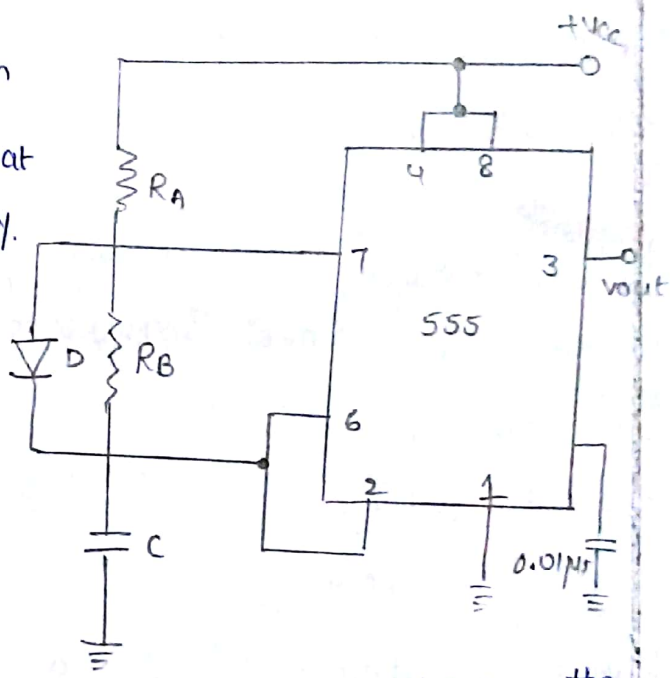
* When flip flop set, Q is high which drives Q_d in saturation and capacitor gets discharged. Now the Capacitor voltage is ntng but trigger voltage. So while discharging less than 1/3 Vcc. and charging path shown by thick Arrows and Totata Resistance in charging path is $(R_A + R_B)$, the charging Time Constant is $(R_A + R_B)\,C$.



Applications:

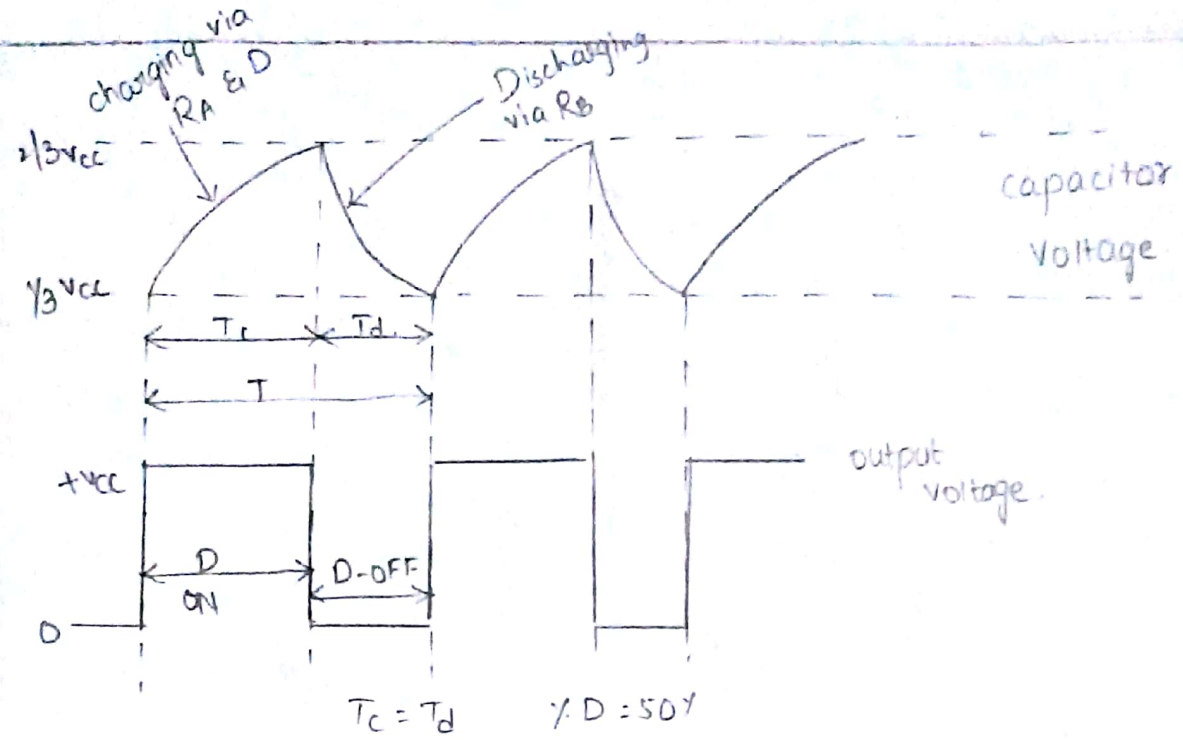
1. Square Wave Generator:

It can be observed from the expression of duty cycle that in astable operation exact 50% duty cycle is not possible to achieve. To get exactly 50% duty cycle i.e., square wave o/p it is necessary to modify the astable Timer circuit.

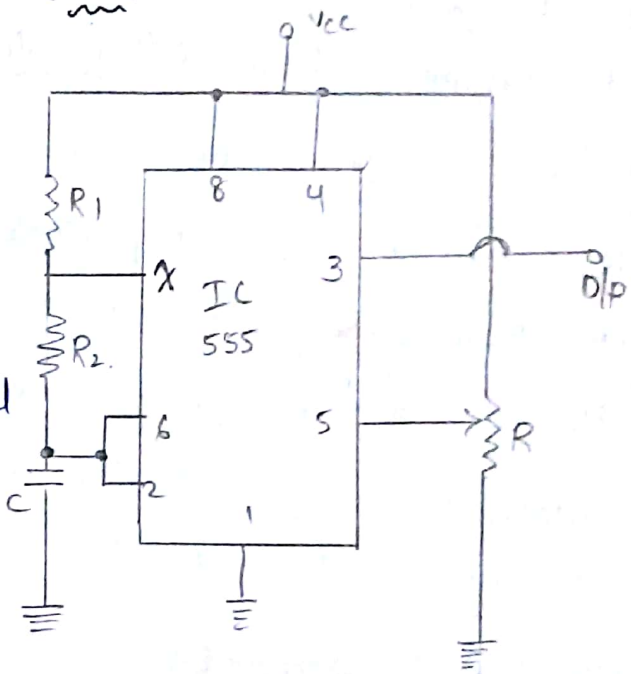


The modified astable CKT used to obtain the square wave o/p shown.

In modified CKT, capacitor C charges through R_A and diode D and discharges through R_B. To obtain square wave (50% duty cycle) R_B adjusted such that it equal to summation of R_A & frwd Res of D.

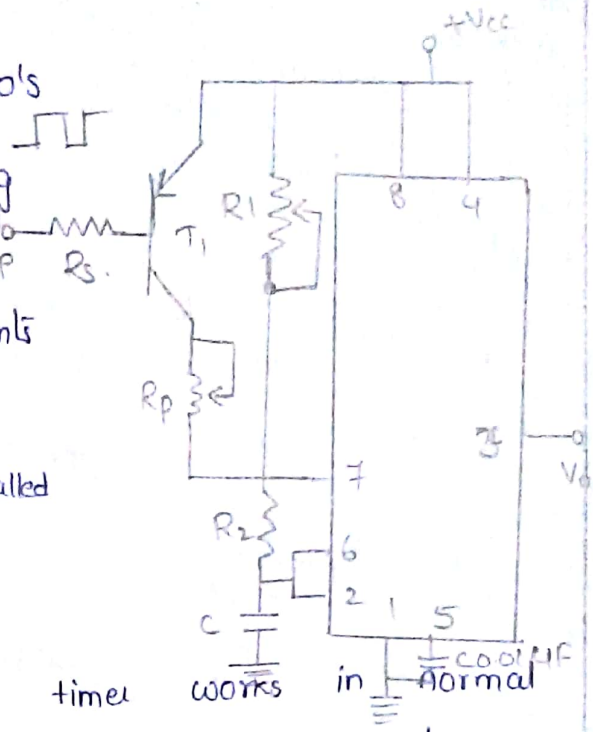


2. Voltage Controlled Oscillator (VCO) :



* It is basically an Astable Multivibrator circuit with variable Control voltage.
* We know that internally set voltage at control voltage terminal is 2/3 Vcc. In this CKT the Control voltage is Externally set by potentiometer.
* If control voltage is increased, capacitor will take more time to charge and discharge and therefore frequency will decrease. On otherhand, if control voltage is decreased the capacitor will take less time to charge and discharge, increasing freq of o/p s/g.
* Thus by varying control voltage we can change the frequency.

FSK Generator :



* Binary code consists of 1's & 0's. It can be transmitted by shifting Carrier frequency. one fix frequency represent one and other represents zero.

* This type of transmission if called Frequency shift Keying Technique.

* When Logic 1, $T_1 \rightarrow$ OFF, 555 timer works in normal astable mode. The freq of o/p waveform can be

$$f_0 = \frac{1.45}{(R_1 + 2R_2)\,C}$$

* When i/p low, $T_1 \rightarrow$ ON and connects R_P in parallel with R_1. With connecting effective R_{left} becomes $R_1 \parallel R_P$ and o/p freq is now given by.

$$f_0 = \frac{1.45}{\left[\left[R_1 \parallel R_P\right] + 2R_2\right] C}$$

Astable Multivibrator with Variable Duty cycle :

Generally, astable mode IC 555 is used to obtain duty cycle between 50% to 100%. But if duty cycle less than 50% is required, the CKT can be modified as below.

The CKT is similar to square wave generator, but instead of connecting diode across fixed R_B it is

across combination of variable R_2 and R_3.

The Resistance R_2 variable and it can be added to R_1 or R_3 to change charging and discharging resistance. Thus variable duty cycle can be achieved.

The charging time for Capacitor is,

$$T_c = (R_1 + \text{part of } R_2)\, 0.693\, C.$$

The discharging Time for Capacitor is,

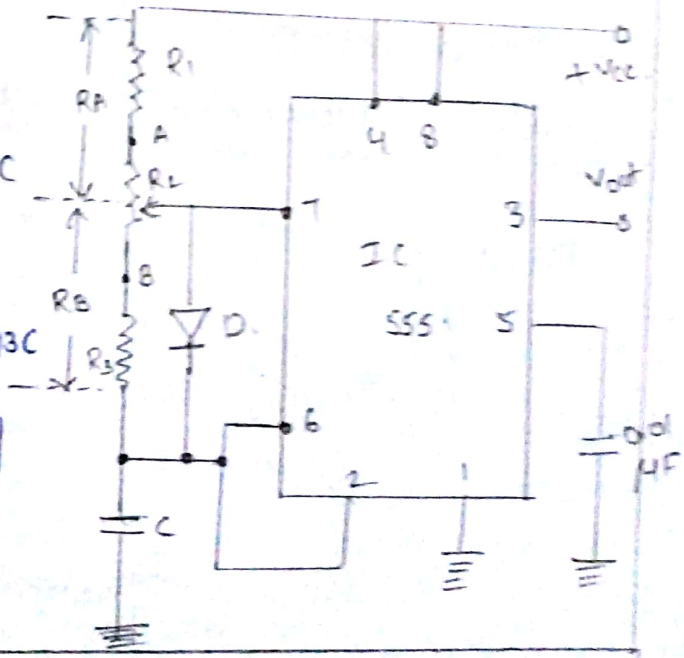
$$T_d = (R_3 + \text{Remaining part of } R_2)\, 0.693\, C$$

$$T = T_c + T_d = 0.693\,[R_1 + R_2 + R_3]\, C$$

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + R_2 + R_3)\, C}.$$

Astable Multivibrator with Variable Duty cycle:

* Generally astable mode of IC 555 used to obtain duty cycle btw 50% to 100%. But if duty cycle less than 50% required, the CKT can be modified.



The charging Time for cap is

$$T_c = (R_1 + \text{part of } R_2)\, 0.693\, C$$

The discharging Time is

$$T_d = (R_3 + \text{Remaining part } R_2)\, 0.693\, C$$

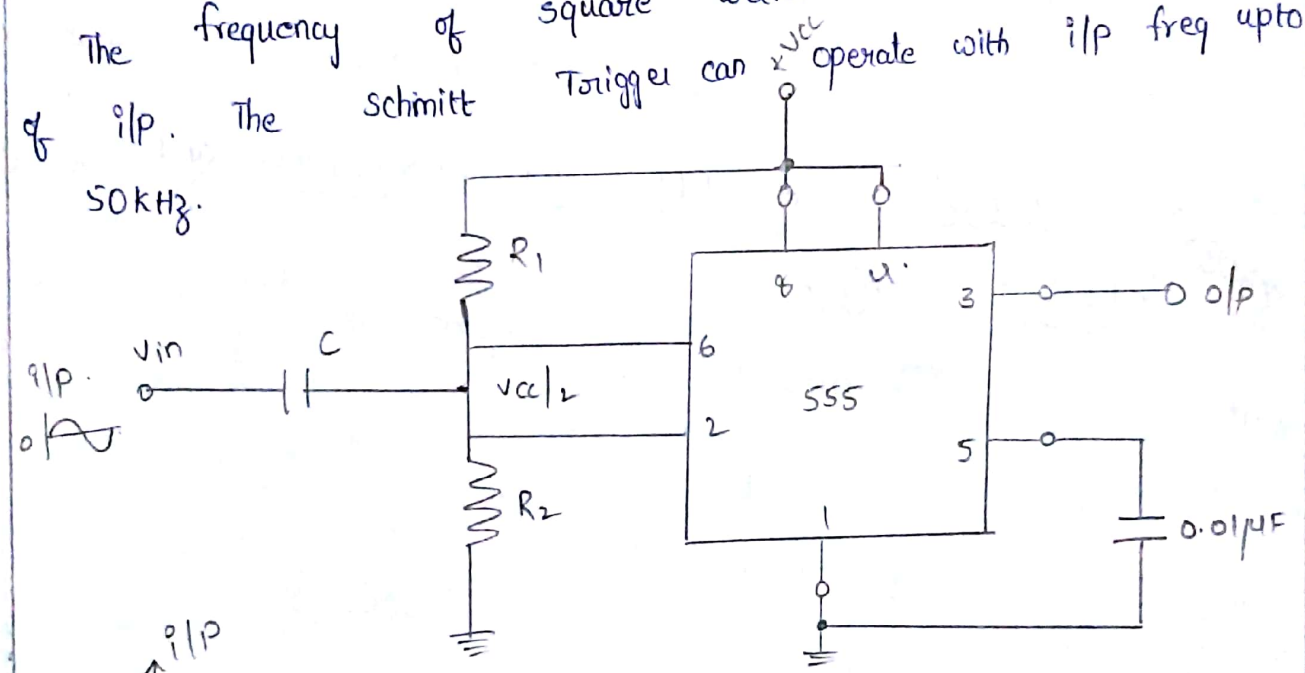
$$T = T_c + T_d = 0.693\, C\,[R_1 + R_2 + R_3]$$

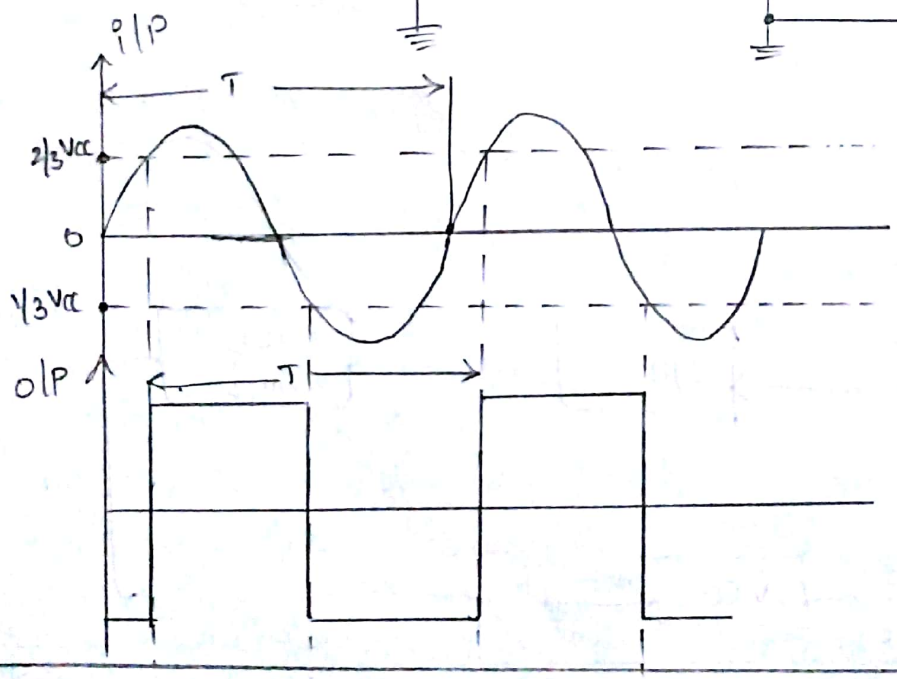
$$f = \frac{1}{T} = 1.44 \,/\, (R_1 + R_2 + R_3)\, C.$$

Schmitt Trigger: using 555 - Timer

The i/p is given to pins 2 and 6 which are tied together. pins 4 and 8 are connected supply voltage $+V_{cc}$. The common point of two pins 2 and 6 is externally biased at $V_{cc}/2$ through the resistance networks R_1 and R_2. Generally $R_1 = R_2$ to get $V_{cc}/2$. The upper comparator will trip at $2/3\ V_{cc}$ while lower comparator at $1/3\ V_{cc}$. The R_1 and R_2 provide bias centred within these two Thresholds.

The frequency of square wave remains same as that of i/p. The Schmitt Trigger can operate with i/p freq upto 50kHz.





PLL - Introduction :

A phase locked loop basically closed loop system designed to lock o/p freq and phase to frequency & phase of i/p signal. It is commonly abbreviated as PLL

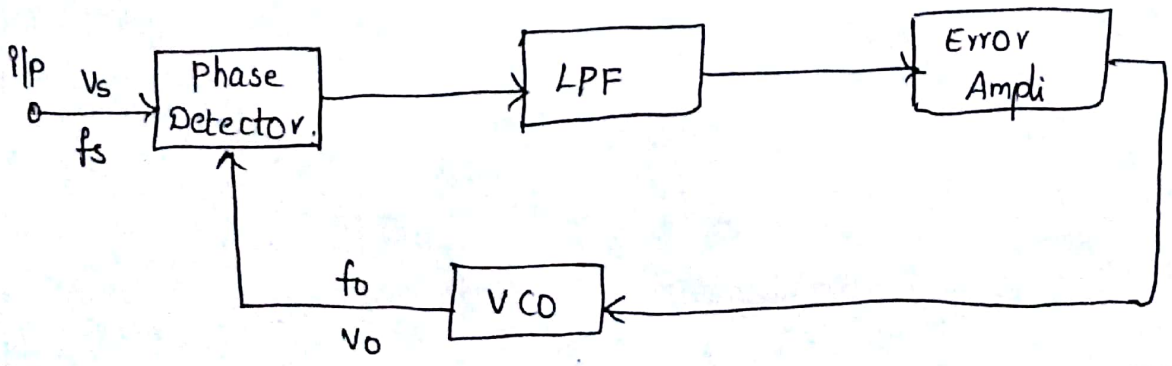
The PLL first introduced in its discrete form early 1930's. The high cost of realizing PLL in discrete form limited its use earlier.

PLL's are available as inexpensive Monolithic ICs. They are used in applications such as freq. synthesis, freq modulation / Demodulation, AM detection, FSK detection etc

Block Schematic of PLL and principles. and Description of Individual block :

The block diagram consists of

1. Phase Detector
2. Low pass filter.
3. Error amplifier.
4. Voltage Controlled Oscillator (VCO)



* The phase detector compares i/p freq (f_s) with the f_o and generates an o/p s/g which is function of difference between the phase of two i/p signals. The o/p s/g of phase detector is dc voltage.

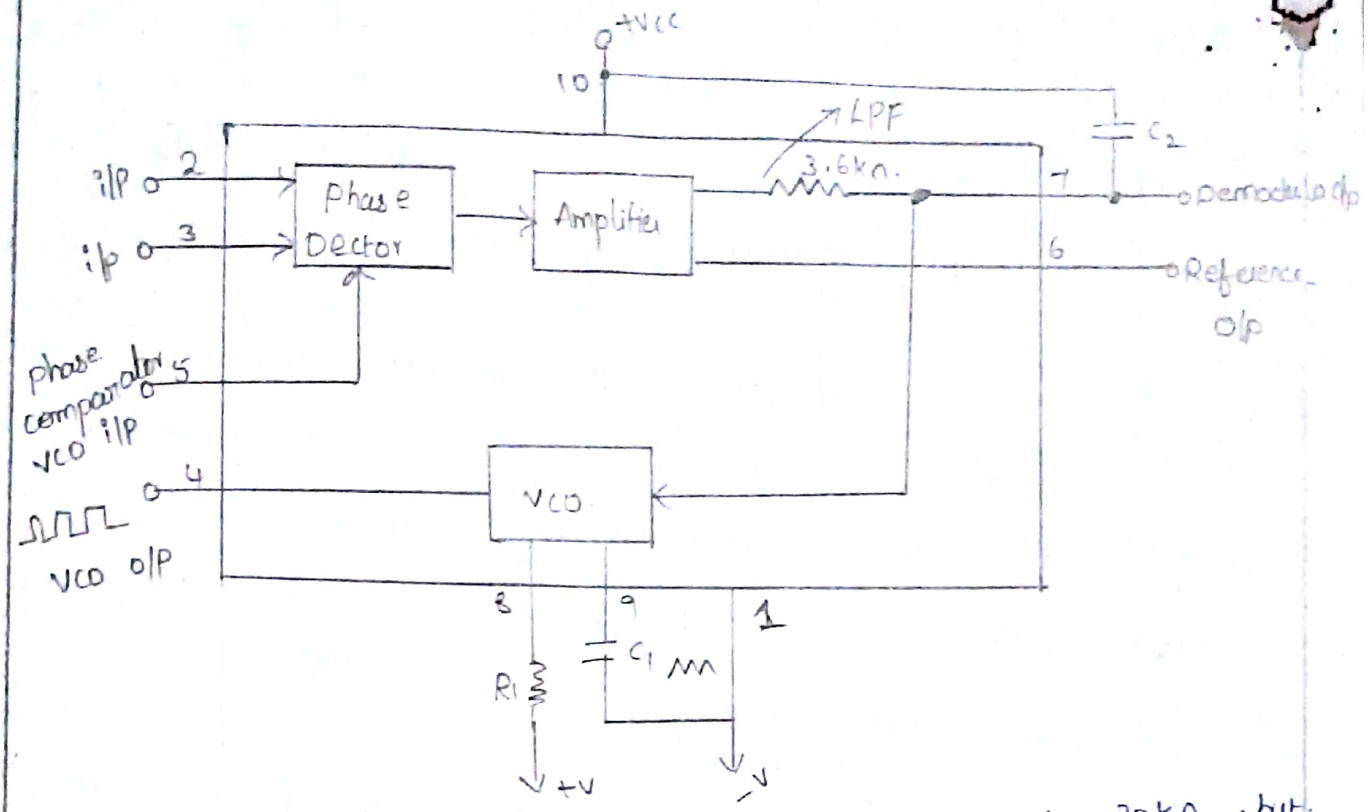
* A VCO is oscillator CKT in which frequency of the oscillation can be controlled by an externally applied voltage. The VCO provides linear relationship between the applied voltage and oscillation frequency. Applied voltage is called Control voltage.

* When Control voltage is zero, VCO is free-running mode and its o/p freq is called Centre frequency.

* The action, commonly known as Capturing, continues till o/p freq of VCO is same as i/p s/g frequency. once two frequencies are same the CKT is said to be locked. In locked condition, phase detector generates a constant dc level which required to shift o/p freq of VCO from Centre freq to i/p freq.

565 PLL :

* Where R_1 and C_1 are an External resistor and Capacitor connected to pin 8 and pin 9, respectively. The values R_1 and C_1 are adjusted such that free running frequency will be at centre of i/p Range.



The value of R_1 restricted from $2k\Omega$ to $20k\Omega$, but capacitor can have value. A C_2 connected between pin 7 and +ve supply (pin 10) forms first order LPF with an Interval resistance of $3.6k\Omega$

The Lock Range and Capture range for IC 565 PLL is given by Eq^n is :

$$f_L = \pm \frac{8 f_o}{V} \text{ Hz} \quad \text{—— (1)}$$

Where $f_o \rightarrow$ free running freq VCO in Hz.

$V = +V - (-V)$ volts.

$$f_C = \pm \left[\frac{f_L}{2\pi (3.6k) C_2} \right]^{1/2} \quad \text{—— (2)}$$

$C_2 \rightarrow$ Farads.

The centre frequency PLL is determined by free running frequency of VCO is given as

$$f_o = 1.2 / 4 R_1 C_1 \text{ Hz} \quad \text{—— (3)}.$$

PLL – Applications :

1. Frequency Multiplier :

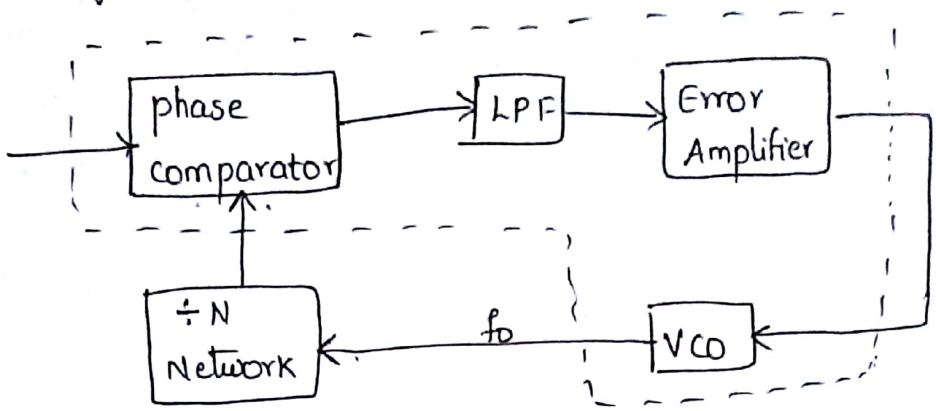
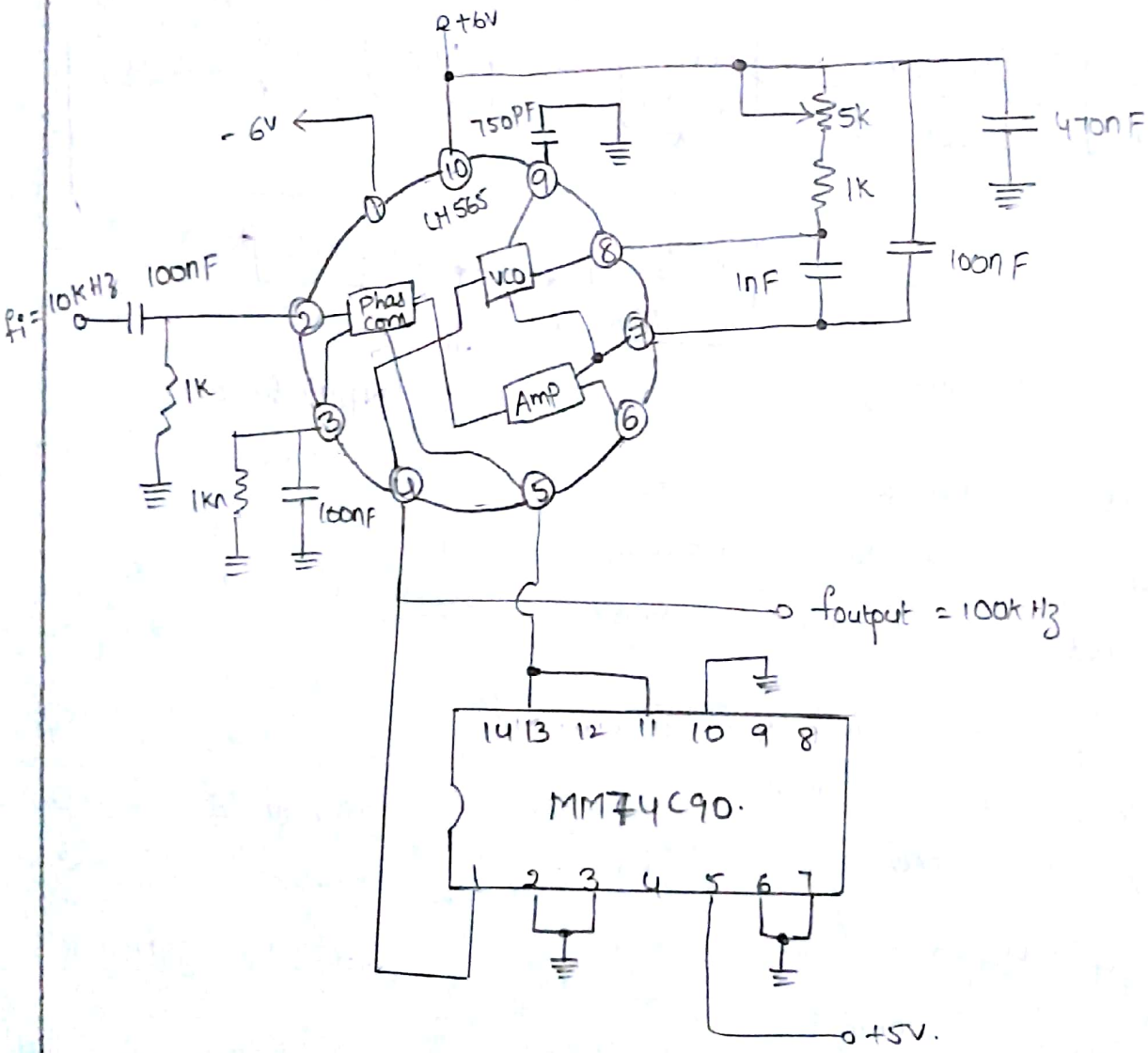


Fig: Block diagram of Freq. Multiplier.



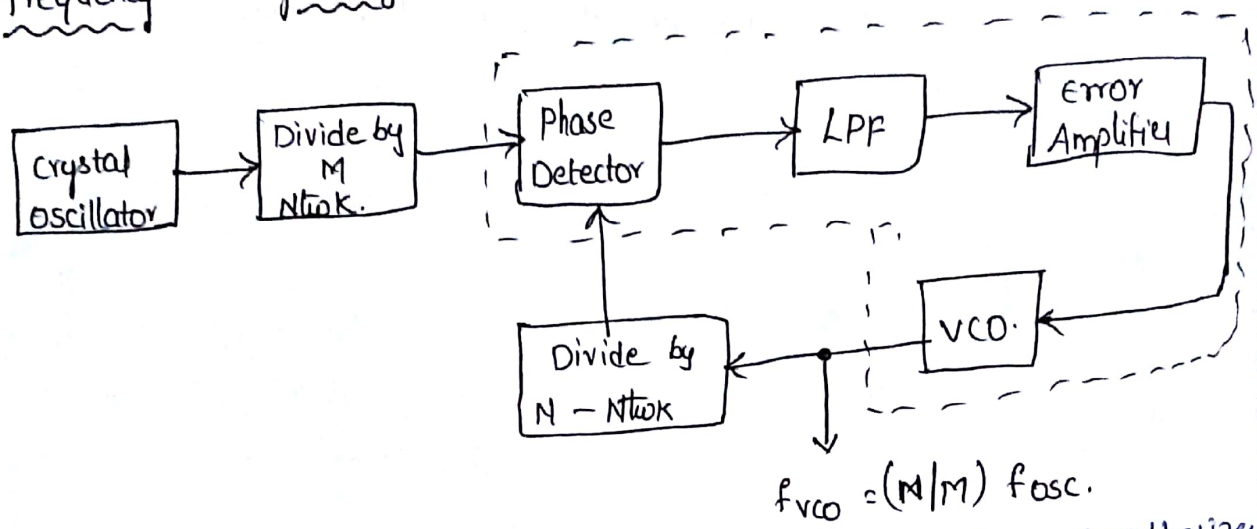
Typical Connection for freq. Multiplier.

* The block diagram, the divide by N - Network, is inserted between VCO output (PIN-4) and phase comparator input (PIN-5). Since o/p of divider is locked to i/p frequency f_i, the VCO actually running at multiple of i/p frequency.

* Therefore in locked state, VCO o/p freq f_o given by

$$f_o = N f_i \quad \text{——— (1)}.$$

frequency Synthesizer:



* The PLL can be used as basis for freq. synthesizer that can be produce precise series of freq. that are derived from stable crystal controlled oscillator.

* The block diagram similar to the frequency multiplier circuit except that divided by M - Network added to i/p of phase lock loop. The freq. of crystal controlled oscillator divided by integer factor M by divider network to produce freq f_{osc}/M where $f_{osc} \rightarrow$ freq of crystal controll oscill

* When PLL is locked in on the divided - down oscillator frequency, we will have $f_{osc}/M = f_{vco}/N$ so that

$$\boxed{f_{vco} = (N/M) f_{osc}}$$

3. FM – Demodulator :

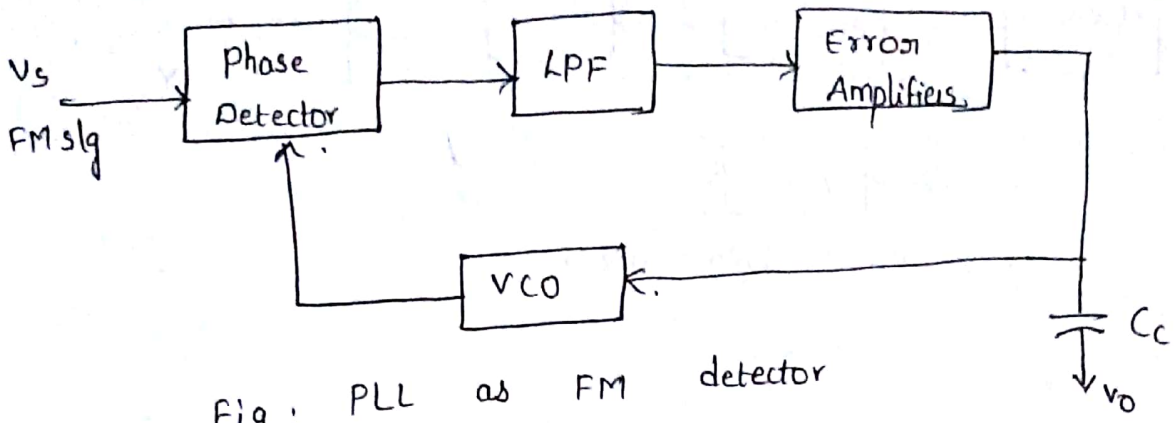


Fig : PLL as FM detector

* The PLL can be very easily used as FM detector. When PLL is locked in on FM signal, VCO frequency follows the instantaneous frequency of the FM signal, Error voltage (or) VCO control voltage is proportional to deivation of i/p frequency from centre frequency.

* Therefore AC – component of voltage (or) control VCO will represent true replica of modulating voltage that is applied to FM Carrier at Transmitter.

* If the product of modulation frequency (fm) and frequency deviation exceeds $(\Delta f_c)^2$, the VCO will not be able to follow the instaneous frequency variations of FM Signal.

4. Frequency Shift Keying (FSK) Demodulator :

* It is Similar to PLL demodulator for analog FM Signals except for addition of comparator to produce a reconstructed digital output Signal.

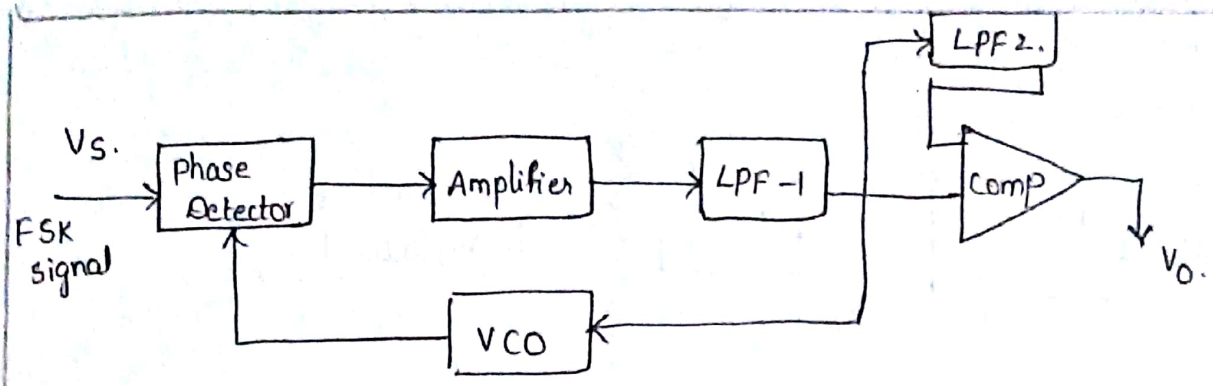


Fig: FSK – Demodulator

$V_{C1} = (f_1 - f_0)/K_V$ and.

$V_{C2} = (f_2 - f_0)/K_V$ respectively.

The difference between two control voltage levels will be $\Delta V_C = (f_2 - f_1)/K_V$.

AM – Detection:

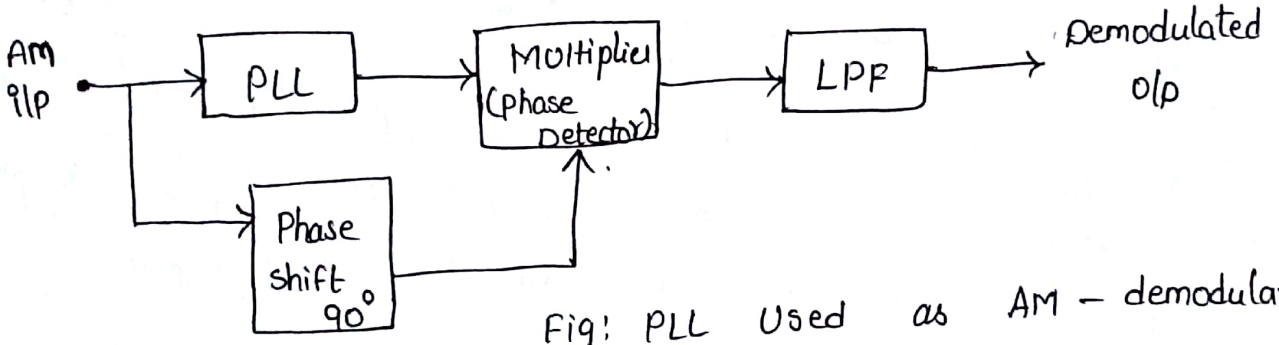


Fig: PLL Used as AM – demodulator.

* A PLL can be used to demodulate AM signals The PLL is locked to carrier frequency of incoming AM signal. Once locked the o/p freq of VCO is same as carrier frequency, but it is in unmodulated form.

* The modulated signal with 90° phase shift & unmodulate carrier from o/p of PLL are fed to multiplier. Since VCO o/p is always 90° out of phase with incoming AM s/g under locked condition, both s/g's applied to multiplier are same phase. The LPF at o/p of multiplier rejects high frequency components and gives demodulated output.

Frequency Translation:

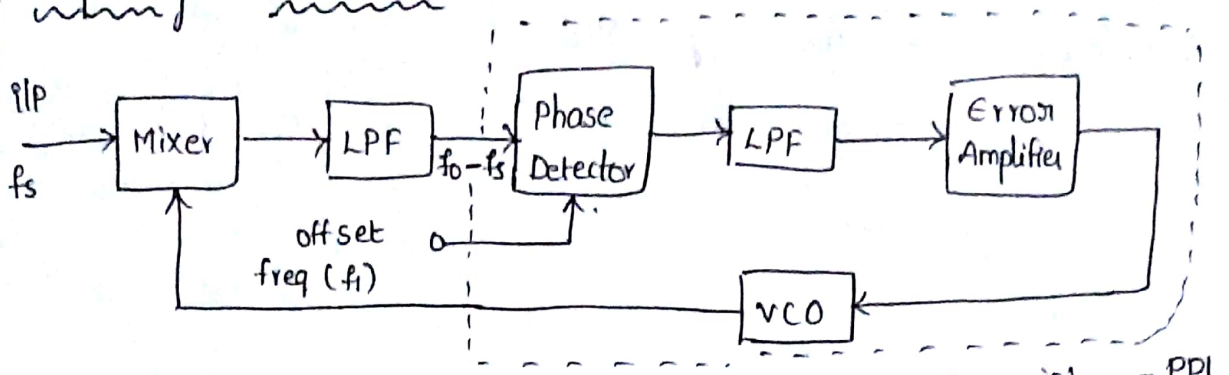


Fig: Block schematic for frequency Transistor - PPL

* The frequency Translation means shifting freq of an Oscillator by small factor.

* It consists of mixer, LPF and PLL. The i/p freq (fs) which has to be shifted applied to mixer. Another i/p to mixer is o/p v/tg of VCO, fo.

* Therefore o/p of mixer contain sum and difference s/g (fo ± fs). The LPF o/p rejects (fo + fs) and gives (fo - fs)

$$f_o - f_s = f_1$$

$$f_o = f_s + f_1$$

* By adjusting offset freq f_1 we can shift freq of Oscillator to desired value.

Applications of VCO:

1. FM Modulation
2. Signal Generation (Triangular / square wave)
3. Function Generator
4. Frequency Shift Keying i.e., FSK demodulator.

5. In Frequency Multiplier:

6. Converting low freq slg such as EEG and EKG into audio freq range slg's.

7. Tone Generation

UNIT - VI

DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS :

Introduction :

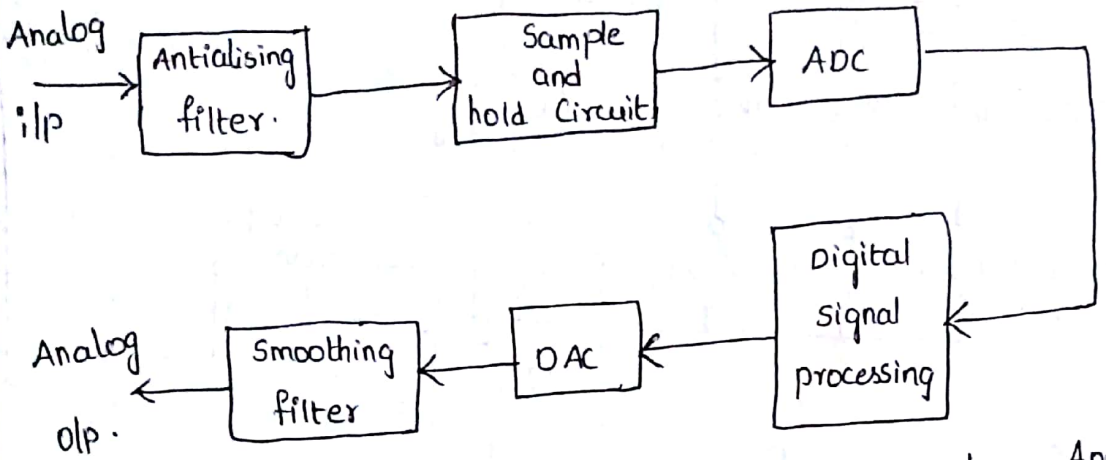


Fig : Typical A/D and D/A Converter Applications.

* Most of information carrying signals such as vltg, current, charge, Temp available in analog form. Moreover, development in microprocessor Technology has made it compulsory to process data in digital form.

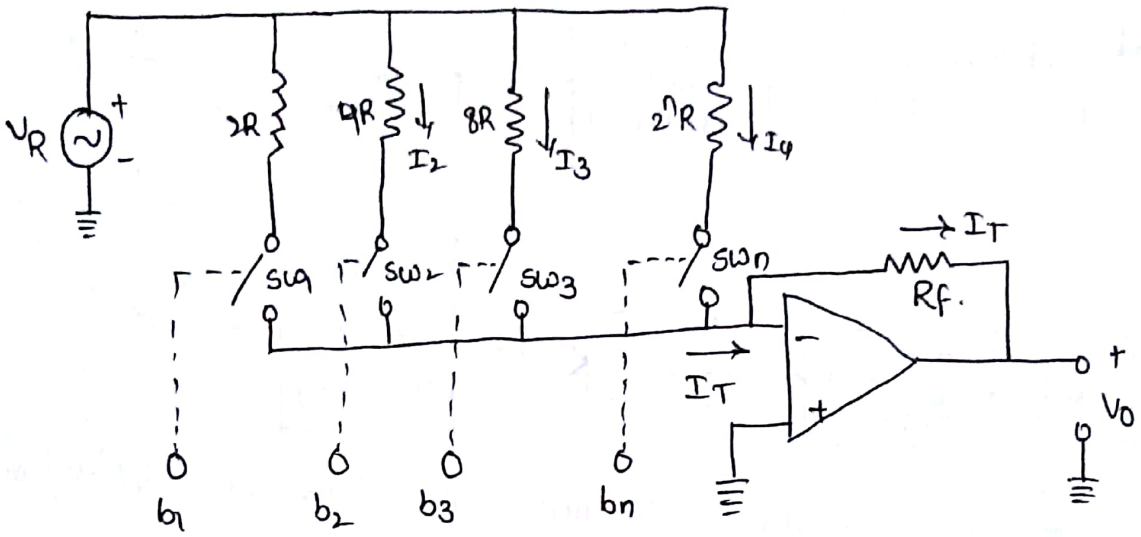
* Since digital system such as microprocessor use binary system of one's and zero's we have to convert signal from analog form to digital.

* On the other hand, D/A converter used when binary o/p from digital system must be converted to some equivalent analog voltage / current. The system to be controlled required Analog signal. Hence in between computer & system to be controlled the D/A converter.

Basic DAC Techniques:

1. Binary Weighted Resistor D/A Converter:

The binary weighted Resistor DAC uses OP-Amp to sum n-binary weighted currents derived from Ref voltage (V_R) via current scaling resistors. 2R, 4R, 8R, ... $2^n R$ as shown



Binary Weighted Resistor DAC

When digital i/p is logic-1, it connects corresponding resistance to Ref. voltage V_R; otherwise it leaves resistor open.

For ON-switch $I = V_R/R$ —— ①

OFF-switch $I = 0$. —— ②

$$I_T = I_1 + I_2 + I_3 + \dots + I_n \quad \text{—— ③}$$

$$V_0 = -I_T R_f = -(I_1 + I_2 + I_3 + \dots + I_n) R_f$$

$$= -\left[b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right] R_f$$

$$= -\frac{V_R}{R} R_f \left[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n} \right] \quad \text{—— ④}$$

When $R_f = R$, then v_o is

$$V_o = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n} \right) \quad \text{— (5)}$$

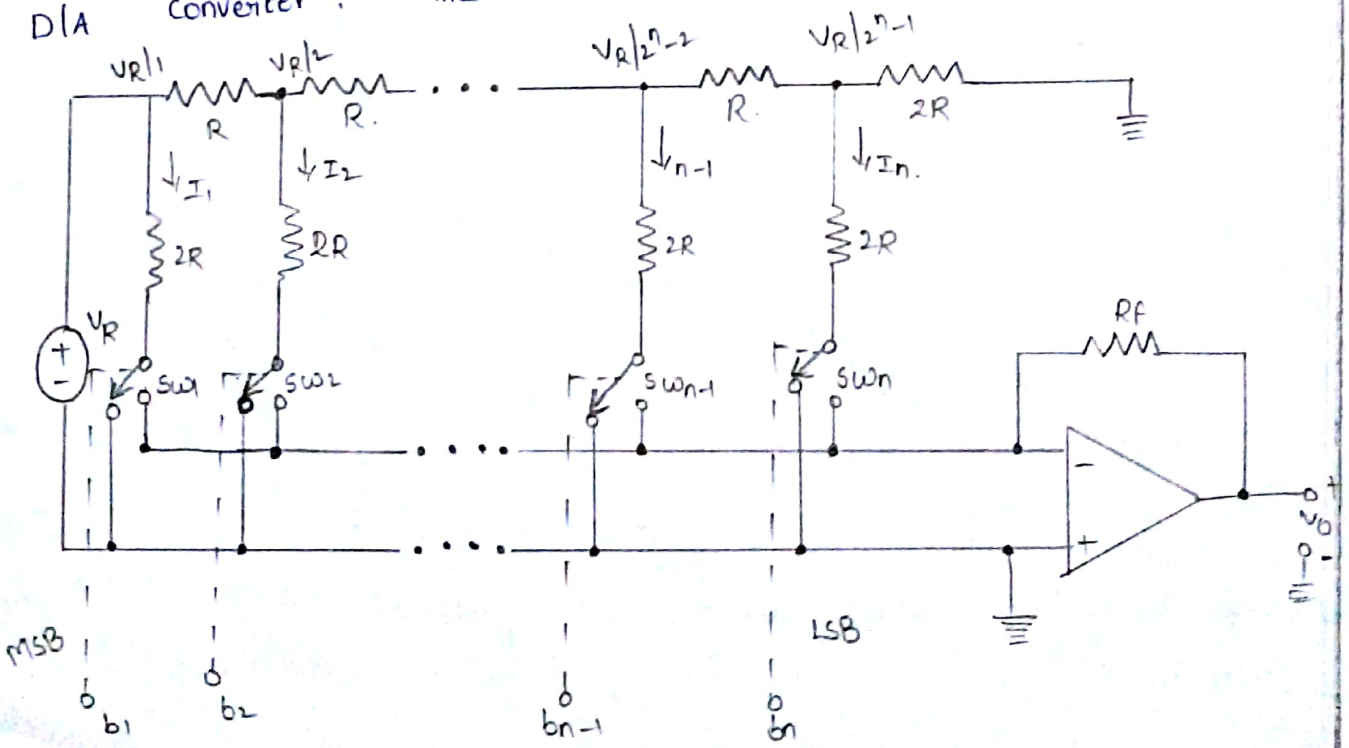
Draw Backs :

1. Wide Range of resistor values are Required. For 8-bit DAC resistors are required $2^1 R, 2^2 R, 2^3 R, \dots 2^8 R$ Therefore largest resistors is 128 times the smallest one

2. This wide range of resistor value has restricitions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across Such large resistor due to bias currents also affects accuracy.

Inverted R/2R Ladder [current steering Mode] D/A Converter

R/2R ladder D/A converter uses only two resistor values This avoids resistance spread drawback of binary weighted D/A converter. The below fig shows R/2R ladder DAC.



$$I_1 = \frac{V_R}{2R} \quad \text{——} \; (1)$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2} \quad \text{——}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}} \quad \text{——} \; (2)$$

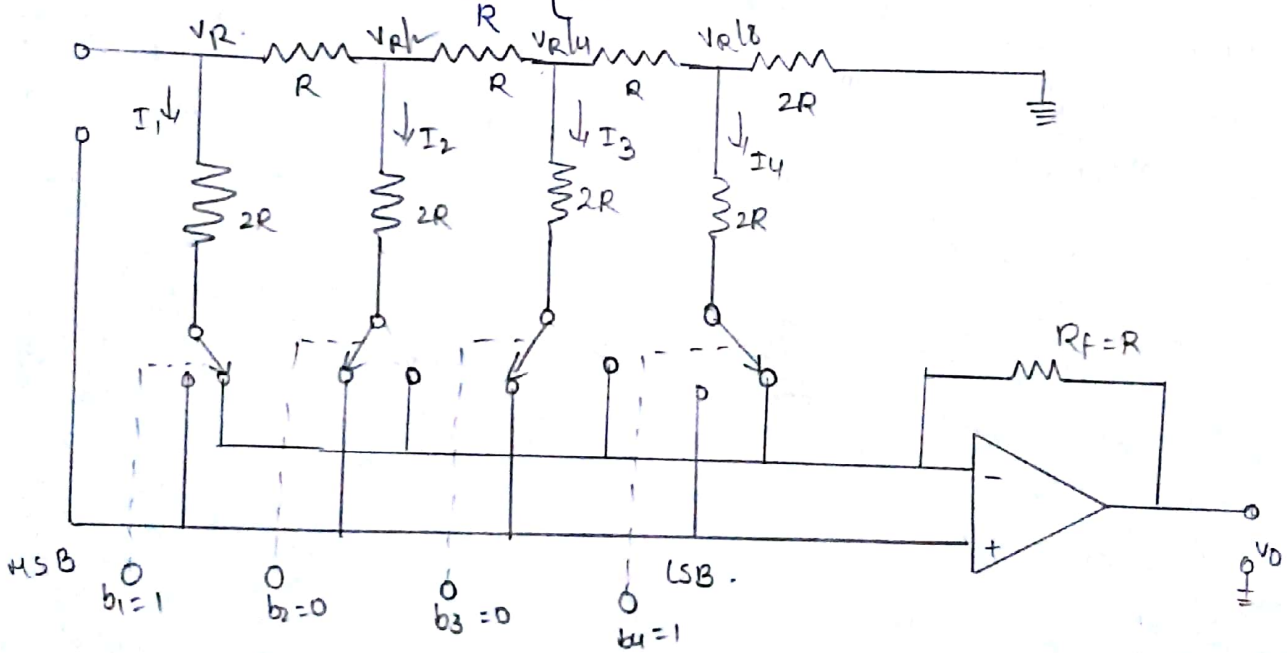
We know that V_o is given as

$$V_o = -I_T R_f \quad \text{——} \; (3)$$

$$V_o = -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -R_f \left[b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right]$$

$$= -\frac{V_R R_f}{R} \left[b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n} \right]$$



$$V_o = -V_R\left(\frac{1}{2} + 0 + 0 + \frac{1}{16}\right) = -0.5625\, V_R = 2.8125\ V.$$

* The inverting R/2R ladder DAC works on principle of summing currents and it is also said to operate in Current Steering Mode.

R/2R Ladder [Voltage Switching Mode] D/A Converter:

* In this Type Reference vltg applied to one of switch position and other switch position connected GND.

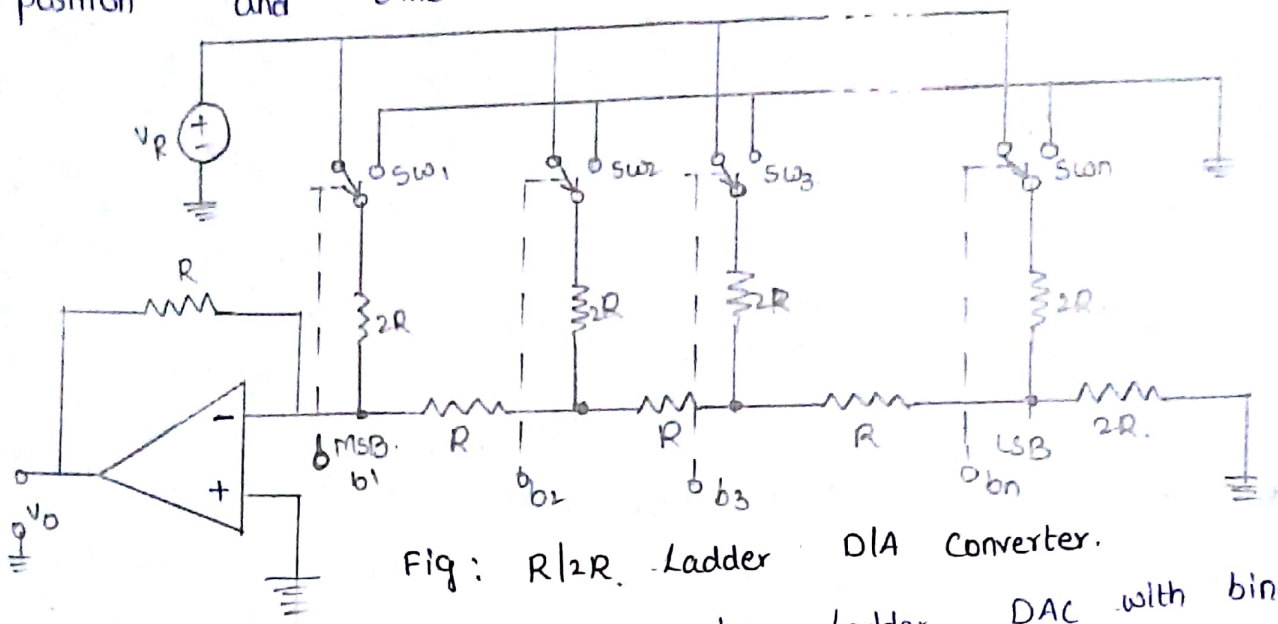


Fig: R/2R Ladder D/A Converter.

* Let us consider 3-bit R/2R Ladder DAC with binary i/p 001 as shown below.

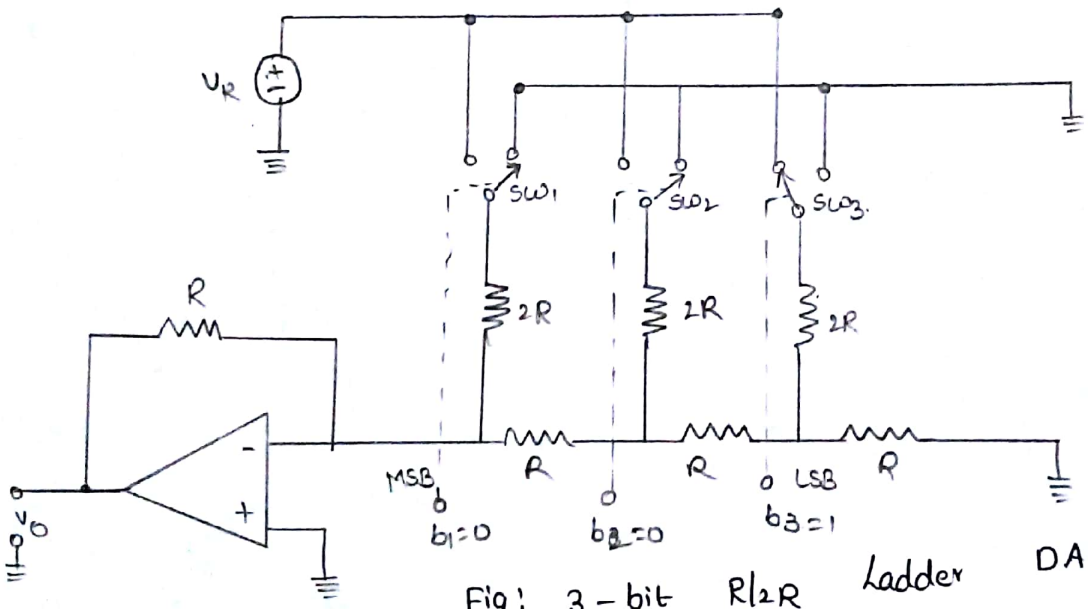


Fig: 3-bit R/2R Ladder DAC.

* Reducing above Network to left by Thevinen's Theorm we get

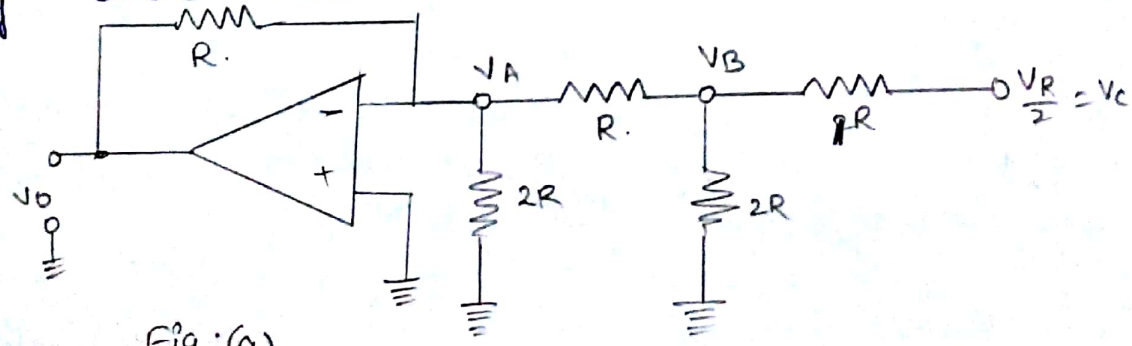


Fig: (a)

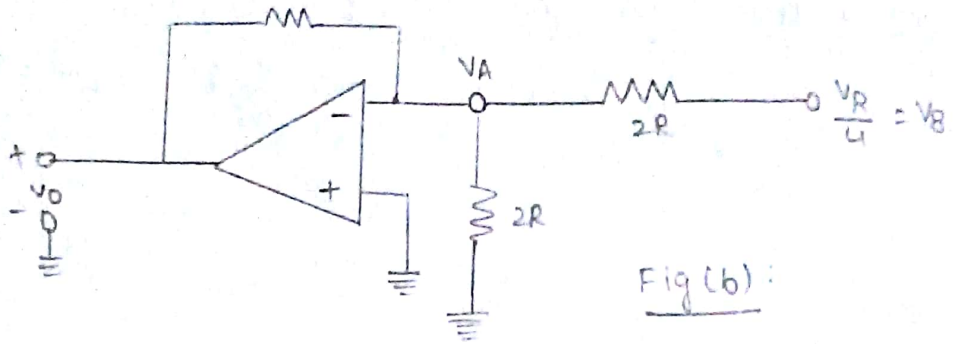


Fig (b):

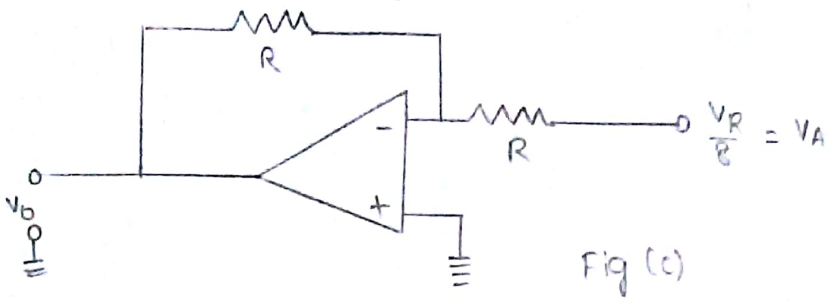
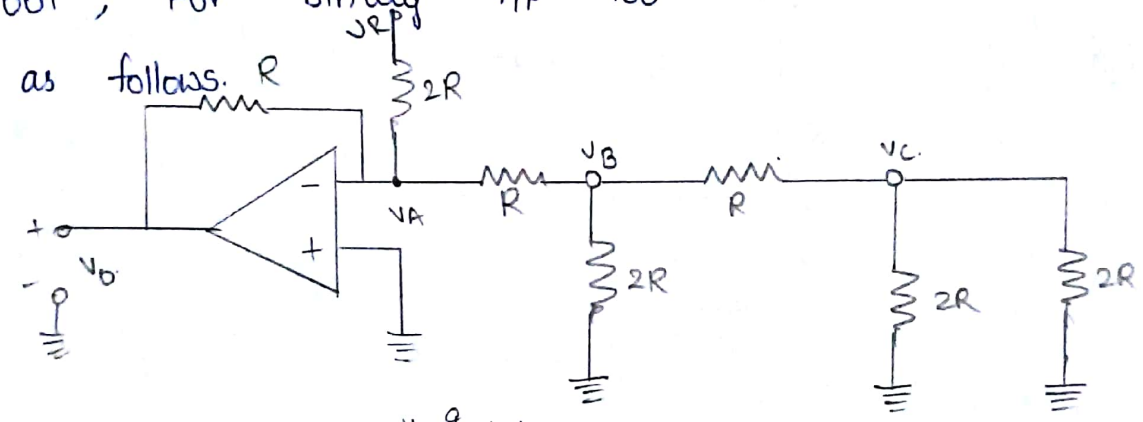
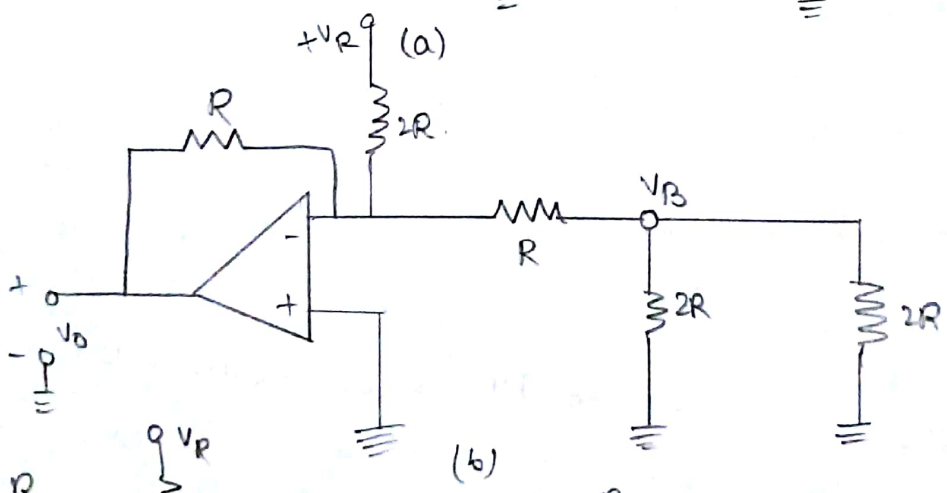


Fig (c)

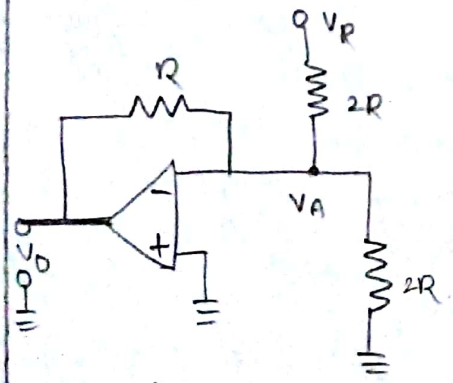
* Therefore o/p voltage $V_R/8$ which Equivalent to binary i/p 001 ; For binary i/p 100 the ntwk can be reduced as follows.



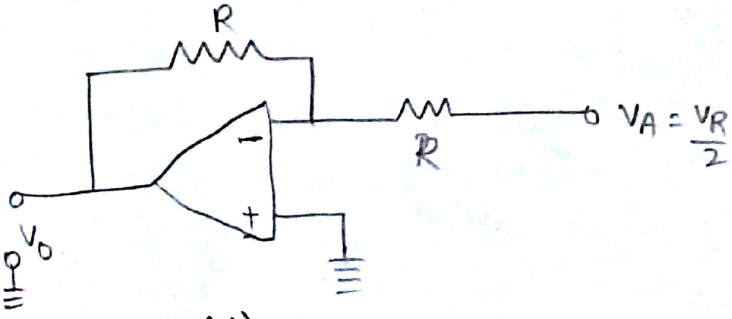
(a)



(b)



(c)



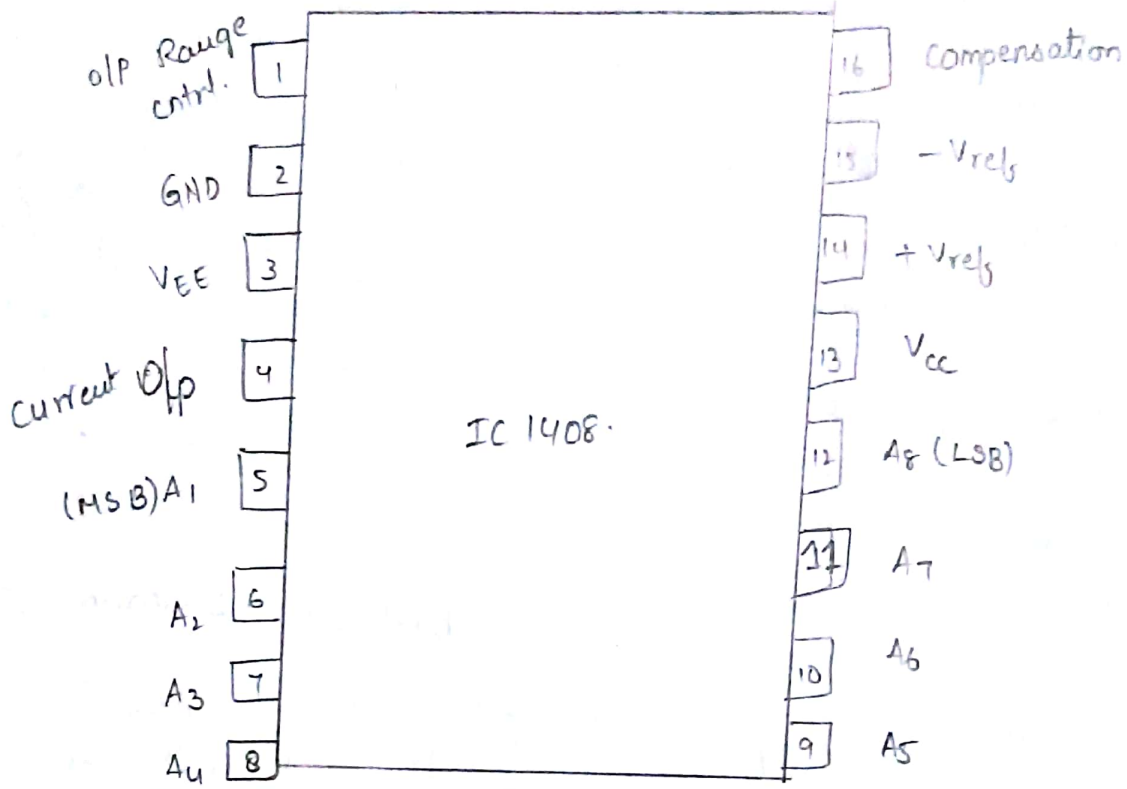
(d)

∴ Therefore, o/p voltage is $V_R/2$, which is equivalent to binary i/p 100.

In general, the voltage given by

$$V_0 = -V_R(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}).$$

IC 1408 DAC :

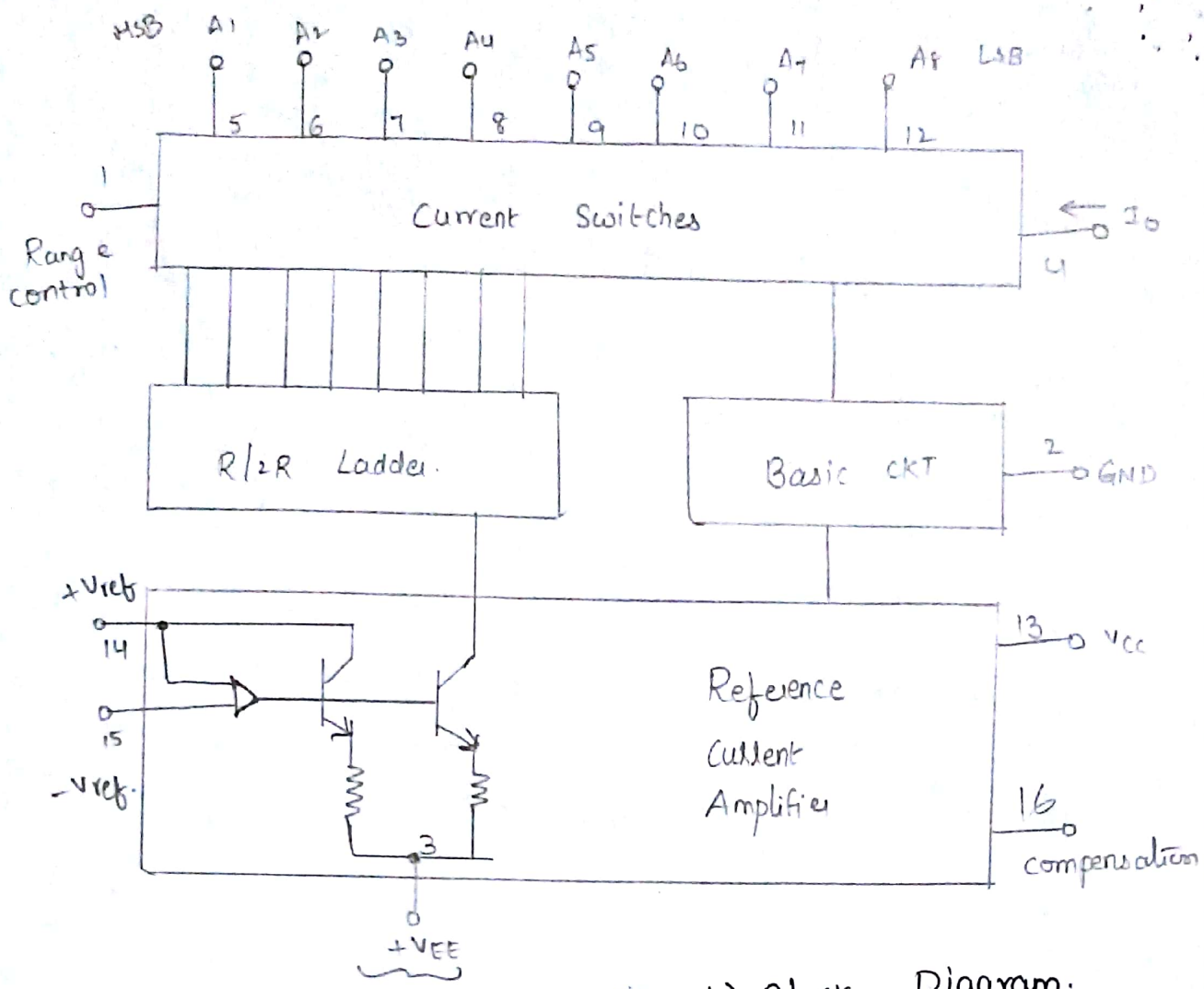


a) PIN Diagram

* The 1408 is an 8-bit R/2R ladder type D/A converter compatible with TTL and CMOS logic. It is designed to use where o/p current is linear product of 8-bit digital word.

* The IC 1408 consists of reference current Amplifier, an R/2R ladder and 8-high speed current switches. It has 8 i/p datalines A_1(MSB) through A_8 (LSB) which cntrol position of current switches.

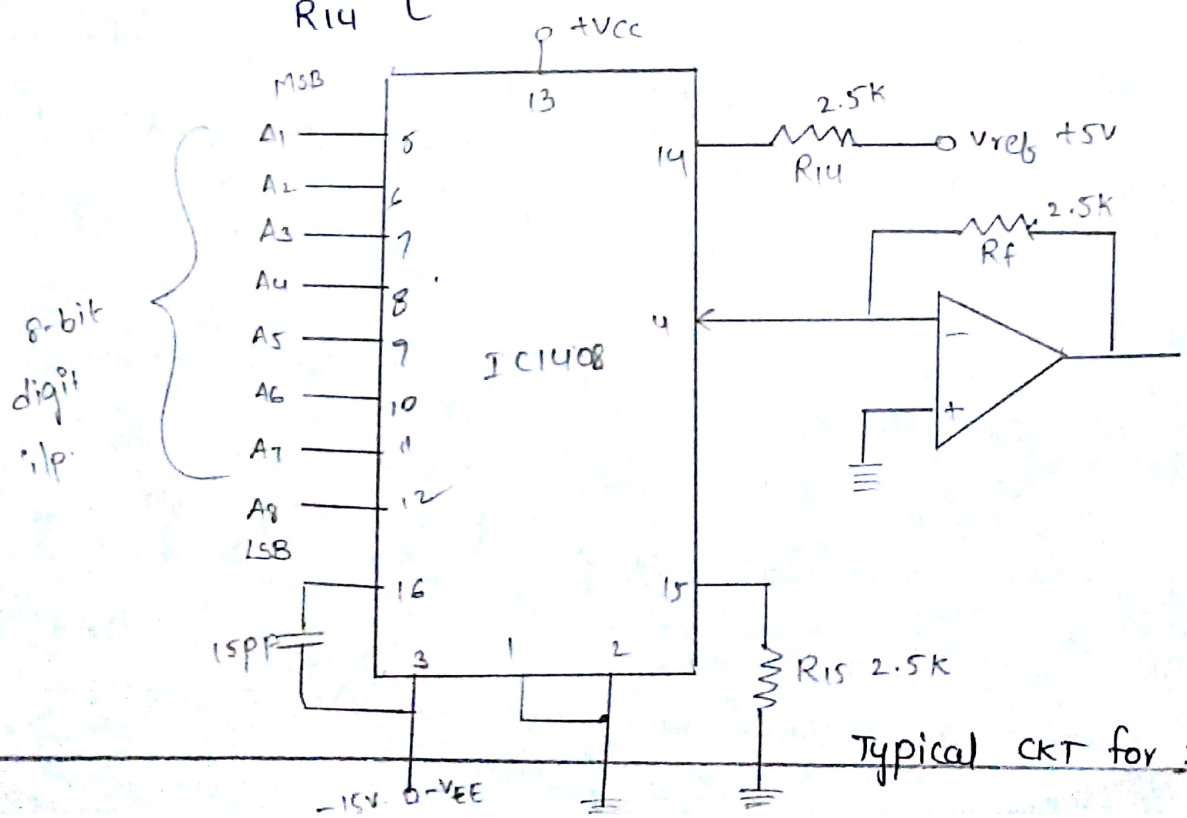
* It require 2mA current & $V_{CC} = +5V$ $V_{EE} = -15V$.



b) Block Diagram.

* The o/p Current (I_0) can given as

$$I_0 = \frac{V_{ref}}{R_{14}}\left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right]$$



Typical CKT for IC1408.

Condition 1 : For binary i/p (00H):

When binary input is 00H the o/p current I_0 at Pin 4 is zero. Due to this current flowing through R_B (1mA) flows through R_f giving $V_0 = -5V$

Condition 2 : For Binary input

When binary i/p 80H the I_0 at pin 4 is 1mA.

By applying KCL at node A. we get

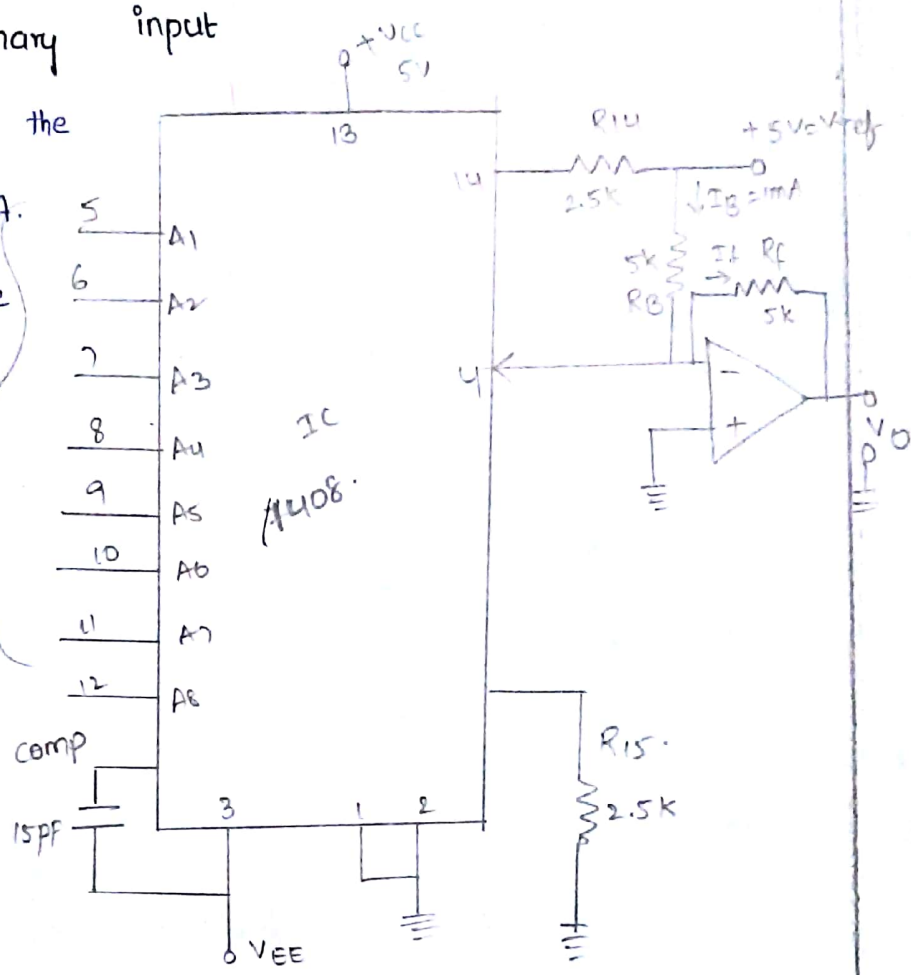
$$-I_B + I_0 + I_f = 0$$

Values I_B & I_0

$$-(1mA) + 1mA + I_f = 0$$

$$I_f = 0$$

Therefore o/p vltg zero.



Condition 3 : For binary input FFH:

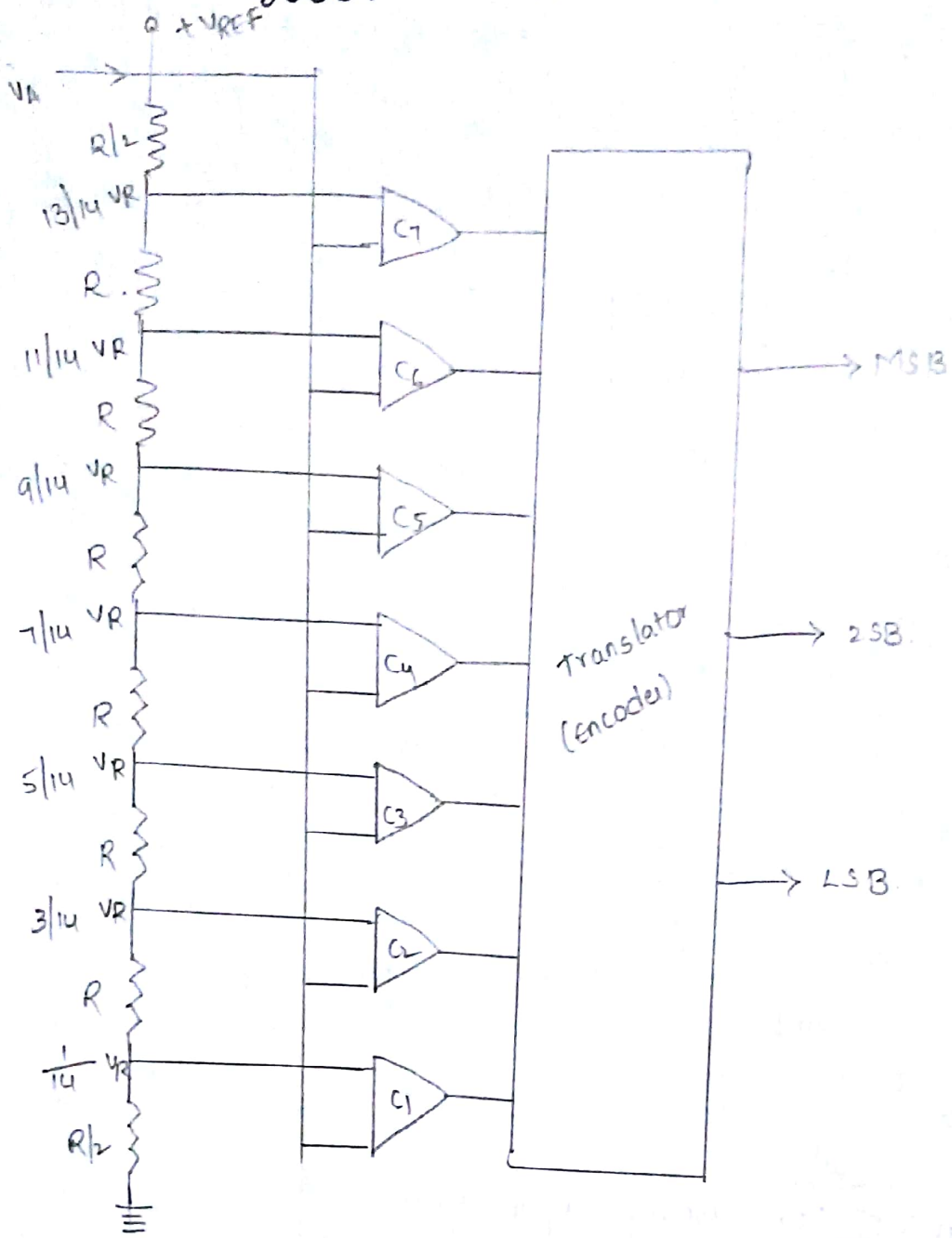
When binary i/p is FFH the o/p current (I_0) at pin 4 at 2mA. By applying KCL at node A we get.

$$-I_B + I_0 + I_f = 0.$$

$$-1mA + 2mA + I_f = 0$$

$$\boxed{I_f = -1mA.}$$

Flash ADC (or) Parallel Comparator ADC :



The Comparator give o/p "1" or "0" state depending on weather the i/p signal is above / below ref level at that instant. Those comparators referred above i/p s/g, remain turned OFF, representing "0" state otherwise "1" state. The code resulting from this comparator converted to binary code by Encoder.

No. of comparators = $2^n - 1$ —— (1)

* As seen earlier quantization Error is $\pm \frac{1}{2}$ LSB Thus for ADC maximum frequency for sine wave Vin to be digitized with in an accuracy of $\pm \frac{1}{2}$ LSB is

$$f_{max} = \frac{1}{2\pi T_c 2^n}$$

where f_{max} = Max. i/p freq

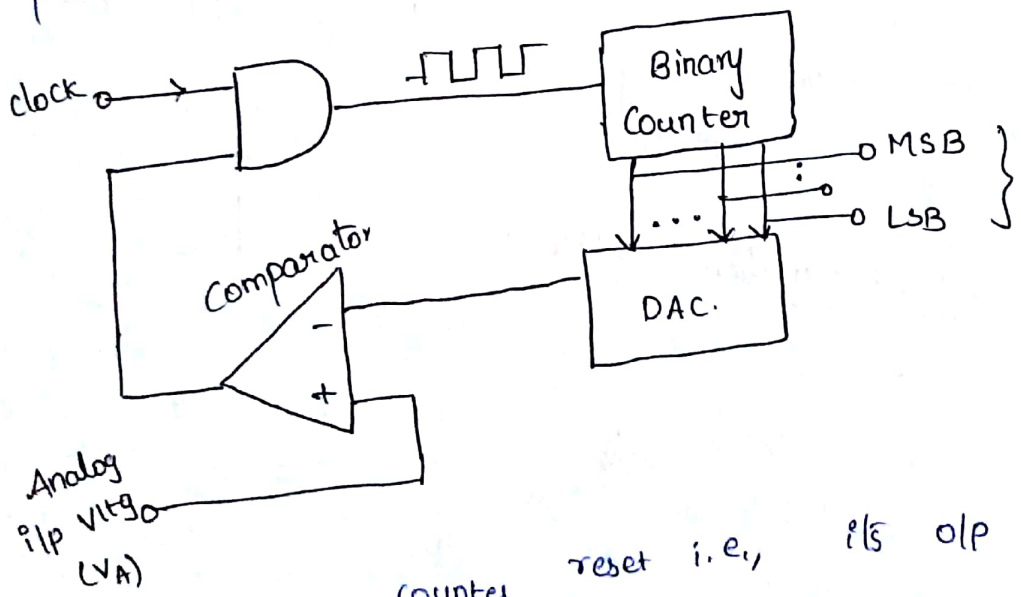
T_c = Conversion Time

n = no. of bits.

Counter Type ADC :

This ADC uses DAC for A to D conversion. The o/p of DAC is continously compared with analog i/p to ADC which is to be converted into digital o/p.

The Counter type ADC consists of binary Counter, DAC Comparator and AND gate operation of CKT explained.



*) Initially, the counter reset i.e., its o/p set to zero by applying reset pulse. The o/p of counter given as digital to DAC. Since i/p to DAC is zero, its o/p V_D is zero.

2) When analog i/p voltage V_A applied to ADC, it becomes greater than V_D. V_A acts as i/p vltg for non-inverting Terminal and V_D acts as i/p vltg for inverting Terminal of comparator.

3) ~~The above~~ For AND gate, one i/p is clock pulse another i/p is o/p of comparator. Because of high o/p of comparator, clock pulses allowed to pass through AND gate.

4) The Counter starts counting these close pulses. According to no. of clock pulses o/p of counter goes on increasing. This increase o/p of DAC.

5) The above steps are continued till V_D is less than V_A.

6) As soon as DAC o/p V_D becomes greater than V_A, the Comparator o/p goes low. This disables AND gate. So clock pulse are not allowed to pass through AND gate. The Counting process of binary Counter is stopped.

Successive Approximation ADC:

* In this Technique, basic Idea to adjust DAC's i/p Code such that o/p within ± 1/2 LSB of Analog i/p (V_1) to be A/D converted. The code that achieves this represents the desired ADC o/p.

* The ADC successive approximation method uses very efficient code searching stategy called Binary Search. It completes Searching process for n-bit Conversion in Just n-clock periods.

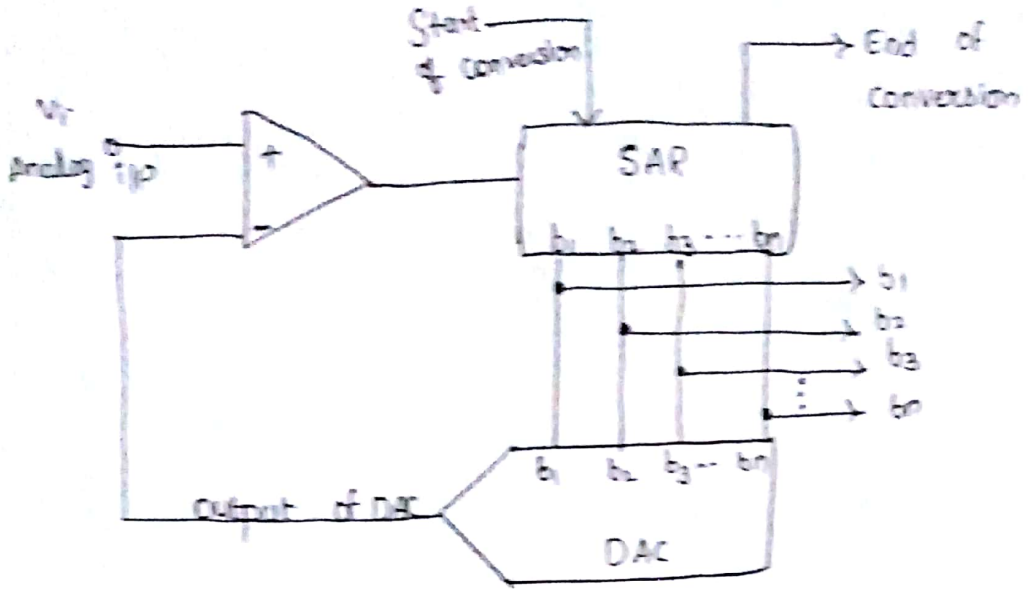


Fig: Block Diagram

* The Searching code process in successive approximation method similar to weighing an unknown material with balance scale and set of standards weight. Let us assume that we have 1kg, 2kg, & 4kg wt (SAR) plus a balance scale.

* The diagram of block and the waveforms. The V_{in} applied at one i/p of comparator. On recieving start of conversion signal successive approximation register sets 3-bit binary code 100_2 ($b_2 = 1$) as an i/p of DAC.

* The clock line the waveforms shows getting & resetting actions of bits for i/p vltg 5.2V, on basis of comparision. It can be seen from fig, that one clock pulse is required for successive approximation register to compare each bit.

* However an additional clock pulse is usually require to reset the register prior to performing conversion.

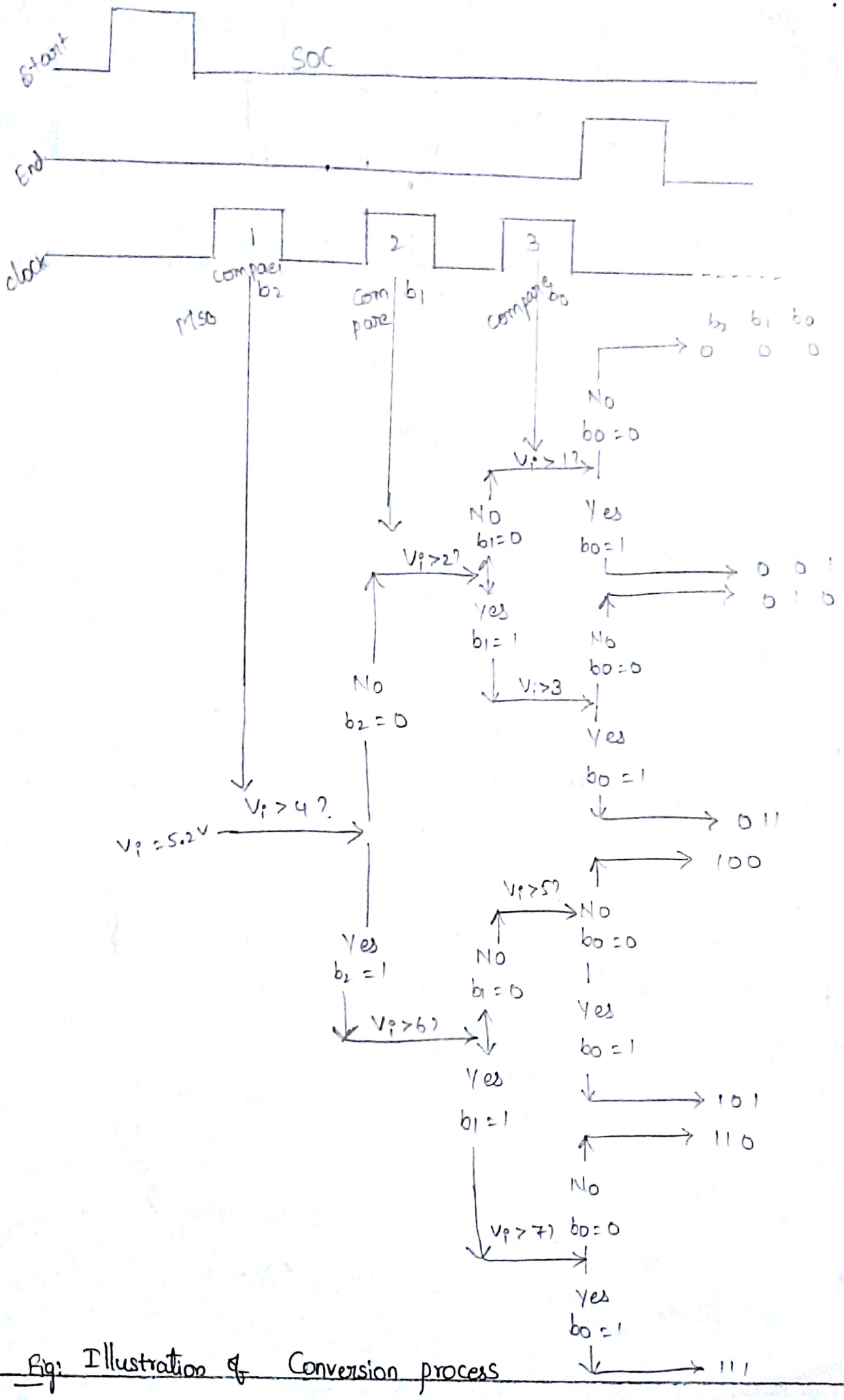


Fig: Illustration of Conversion process

$$T_c = T(n+1) \quad \text{—— (1)}$$

Where $T_c \rightarrow$ Conversion Time

$T \rightarrow$ clock period

$n \rightarrow$ no. of bits.

Dual Slope ADC :

Dual slope ADC where an Analog voltage and Reference voltage are converted into Time periods by an integrator and then measured by counter.

The following figure shows typical dual slope converter circuit. It consists of Ramp Generator, Comparator, binary Counter, Output latch and Reference voltage. The Ramp generator i/p switched between Analog i/p V_i & Negative Ref vltg $-V_{REF}$.

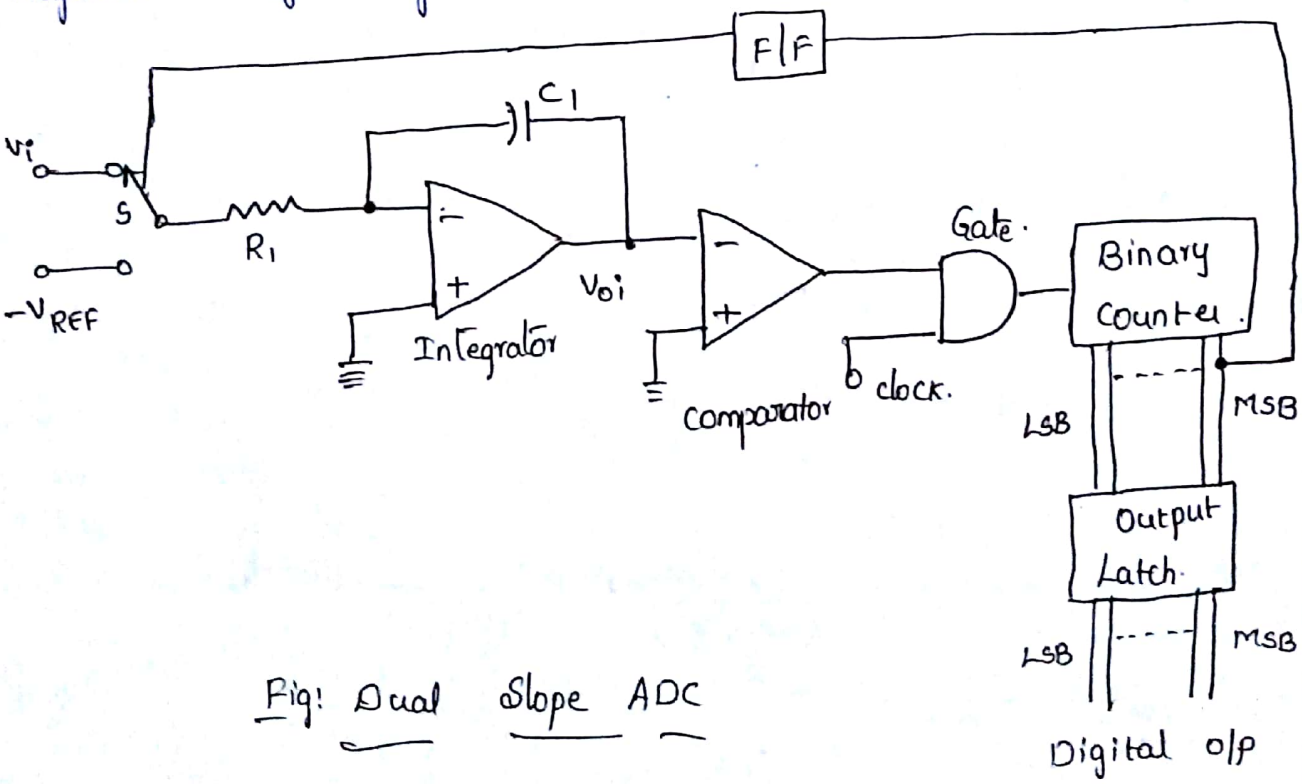


Fig: Dual Slope ADC

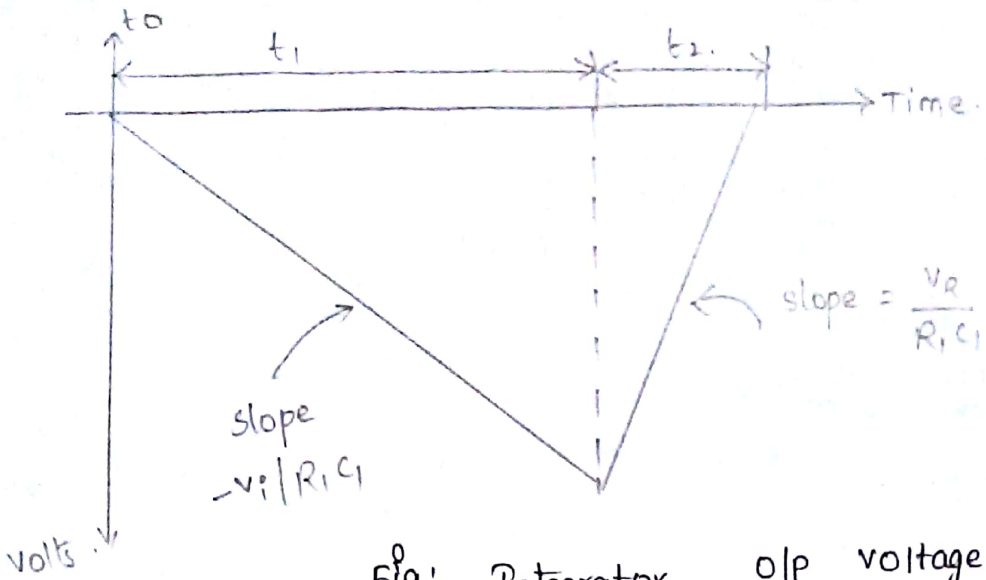


Fig: Integrator o/p voltage.

At $t=0$, Analog switch "S" connected to Analog i/p voltage (v_i) so that Analog i/p vltg integration begins

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t v_i \, dt = \frac{-V_i t}{R_1 C_1} \quad \text{—— (1)}$$

The integrator o/p Ramp down to voltage (v) & get back up to "0". Therefore charge vltg equal to discharge voltage and we can write,

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$t_2 = \frac{V_i t_1}{V_R} \quad \text{—— (2)}$$

$$\text{Digital o/p} = \left[\frac{\text{counts}}{\text{second}}\right] t_2 \quad \text{—— (3)}$$

But from eqn (2)

$$\text{Digital o/p} = \left[\frac{\text{counts}}{\text{second}}\right] t_1 \left(\frac{V_i}{V_R}\right) \quad \text{—— (4)}$$

Dis Advantage:

* Its speed is Low.

Advantage:

1. It is highly Accurate
2. It's cost is low.
3. It is Immune to Temperature caused variation in R_1 and C_1

DAC and ADC Specifications:

Resolution: The resolution of converter is smallest change in voltage with which may be produced at o/p (or i/p) at converter.

* For Eg: 8 bit DAC has $2^8 - 1 = 255$ equal intervals. Hence the smallest change in o/p vltg is (1/255) of full scale o/p range.

$$\text{Resolution in volts} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment}$$

* The Resolution of ADC defined as smallest change in Analog i/p for one bit change as o/p.

Linearity:

The Linearity of ADC/DAC is an important measure of its accuracy and tells us how close the converter o/p is to its ideal T/F characteristics

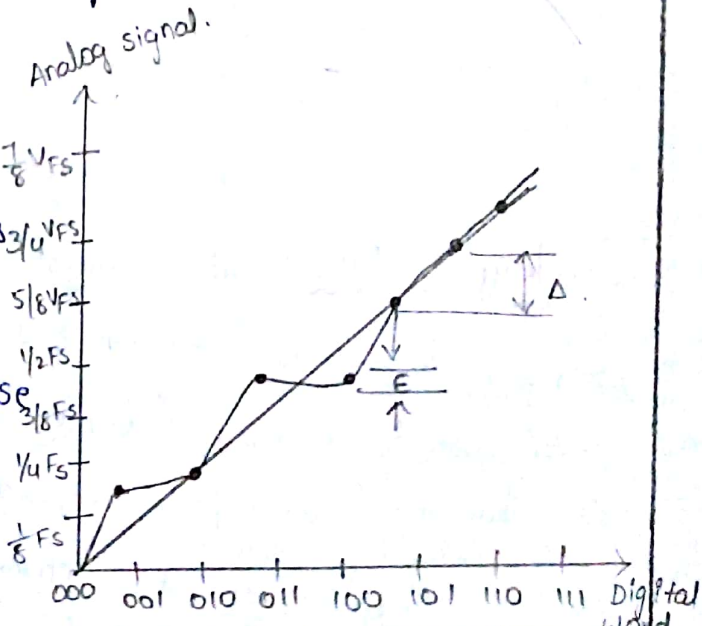


Fig: Linearity Error for 3-bit.

Accuracy: Absolute accuracy is maximum deviation between actual converter o/p and ideal converter o/p. Relative Accuracy is max deviation after gain and offset errors have been removed.

Monotonicity: A monotonic DAC is one whose analog o/p increases for an increase in digital input. The below fig represents T/F curve for non monotonic DAC, since o/p decreases when i/p code change from 001 to 010.

A Monotonic characteristic is essential in control application otherwise oscillations can result. In successive approximation ADC's a non-monotonic characteristic may lead to missi code

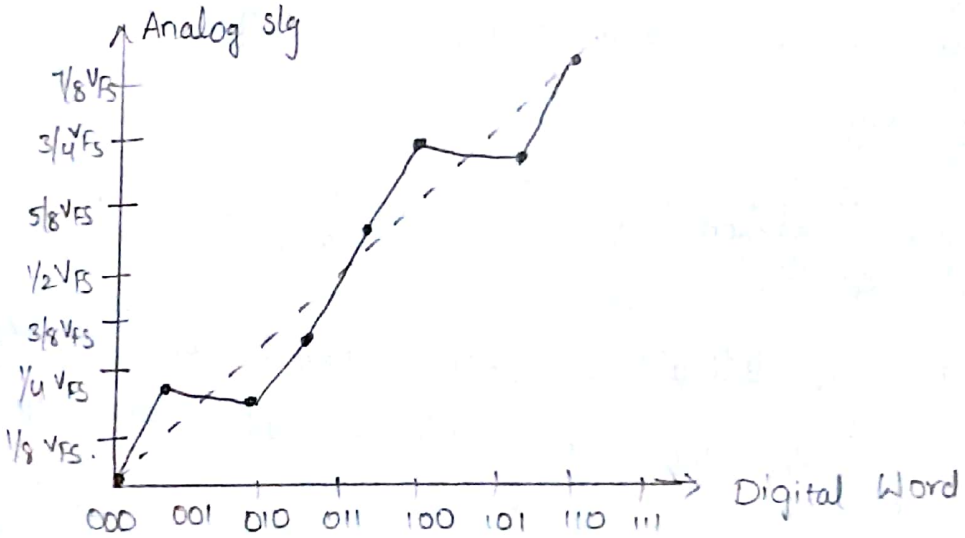


Fig: A Non-Monotonic 3-bit DAC

Settling Time: The most imp dynamic parameter is Settling Time. It represent time it takes for o/p to settle within specified band band ± (1/2) LSB of its final value following code change at i/p. It depends upon switching time of Logic circuitary due to internal parasitic capacitance & inductance.

* Settling Time range from 100ns to 10μs depending on Word length and type of circuit used.

Stability: The performance of converter changes with Temp, age and power supply variations. So all relevant parameter such as offset, gain, linearity error and Monotonicity must be specified over full Temperature and power supply vltg.

AD574A [12-bit ADC] Specification:

* The AD574A is complete 12-bit ADC which requires no external components to provide complete Successive approximation Analog-to-digital Conversion function.

Parameter	Value
Resolution	12-bit
Linearity Error.	±1 LSB
Temperature Range	0-70°c
Analog i/p Range.	-5 to 5V
Power Supply	
V_{Logic}	+4.5 to +5.6
V_{CC}	+11.4 to +16.5
V_{EE}	-11.4 to -16.5
Power Dissipation.	390mW (Typical); 725mW (max)
Internal Reference voltage	9.98 to 10.02
Maximum Conversion Time.	35 μs
operating Current: I_{Logic}	30-40 mA.
I_{CC}	2-5 mA
I_{EE}	18-30 mA.